the application of linear microcircuits volume 2

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THE APPLICATION OF LINEAR MICROCIRCUITS

VOLUME 2

by
the Applications Engineering Staff of SGS

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CONTENTS

Section 1 INTRODUCTION

1.1 Purpose of Handbook

1.2 Instructions for Handbook Usage

Section 2 INTEGRATED CIRCUIT DESCRIPTIONS AND PERFORMANCES

2.1 The L103T2 r.f./i.f. Amplifier

2.1.1 Introduction

2.1.2 Circuit Description

2.1.3 Circuit Performance

2.2 The L123T2 Voltage Regulator

2.2.1 Introduction

2.2.2 Circuit Description

2.2.3 Circuit Performance

2.3 The L127T2 Temperature Controlled Differential Preamplifier

2.3.1 Introduction

2.3.2 Circuit Description

2.3.3 Circuit Performance

2.4 The L141T2 High Performance Operational Amplifier

2.4.1 Introduction

2.4.2 Circuit Description

2.4.3 Circuit Performance

Section 3 LINEAR INTEGRATED CIRCUIT APPLICATIONS

3.1 L103T2 Basic Circuits

3.1.1 100 MHz and 200 MHz RF Amplifiers

3.1.2 FM IF Amplifier

3.1.3 Harmonic Mixer

3.1.4 10 MHz Oscillator

3.2 L123T2 Power Supply Circuits

3.2.1 Basic Low Voltage Regulator

3.2.2 Basic High Voltage Regulator

3.2.3 Positive Voltage Regulator (External NPN Pass Transistor)

3.2.4 Regulator with High Power Supply Rejection

3.2.5 Negative Voltage Regulator

3.2.6 Negative Voltage Regulator

3.2.7 Positive Low Voltage Regulator with remote shut down

3.2.8 Current Regulator

3.2.9 Shunt Regulator

3.3 L127T2 Basic Circuits

3.3.1 Low Drift Operational Amplifier

3.3.2 High Performance Voltage Follower

3.3.3 Precision Integrator

3.3.4 High Input Resistance Comparator

3.4 L141T2 Basic Circuits

3.4.1 Voltage Follower

3.4.2 Integrator

3.4.3 Differentiator

3.4.4 Inverting Amplifier

3.4.5 Non-Inverting Amplifier

3.4.6 Clipping Amplifier

3.4.7 Voltage Comparator

3.4.8 Voltage Regulator Amplifier

1. INTRODUCTION

1.1 PURPOSE OF HANDBOOK

This Handbook has been produced so as to bring under one cover comprehensive details of the linear integrated circuits not described in Volume 1 of 'the application of linear microcircuits'. Reference will be made to Volume 1 to avoid duplication of existing information.

Practical circuits have been included with component values but, due to the many applications that are possible, supplementary notes are included. By this means and the general information available in Volume 1 it is hoped that the engineer will be in a position to design circuits to his specific requirements.

1.2 INSTRUCTIONS FOR HANDBOOK USAGE

It will be noted that the contents are divided into Sections and Sub-Sections which are identified by means of a two-or three-digit code.

The location of any of the specified material shown in the 'List of Contents' pages can therefore be readily found. The date of issue is indicated at the foot of the second page.

The Company should be consulted to obtain the latest information available concerning the Linear Integrated Circuit Family.

Unless otherwise specifically stated, the pin numbers shown in various circuit diagrams refer to the TO–5 package. For the connections applicable to alternative packages, the appropriate data sheet should be consulted.

2. INTEGRATED CIRCUIT DESCRIPTIONS AND PERFORMANCES

2.1 The L103T2 r.f./i.f. Amplifier

2.1.1 Introduction

The r.f./i.f. amplifiers and mixers in most receiving systems generally employ few components in addition to the tuned circuits. Since tuned circuits cannot be economically integrated with existing technology, use of the remaining components in integrated form is worthwhile only if a substantial improvement in performance or stability can be obtained or if simplified design procedures can be used.

These improvements are provided by the emitter-coupled amplifier shown in Figure 2.1.1. Designed for use with transformers and/or tuned circuits the L103T2 eliminates the biasing resistors, bypass capacitors, and coupling capacitors required in conventional amplifiers. Operation is essentially unilateral, and the circuit has a symmetrical output current limiting characteristic. This provides increased available power gain, simplified tuning, and superior limiting performance which greatly reduces the detuning, phase shift and blocking that occur when conventional amplifiers saturate. The device may also be used as a harmonic mixer and is especially attractive when used as an FM limiter.

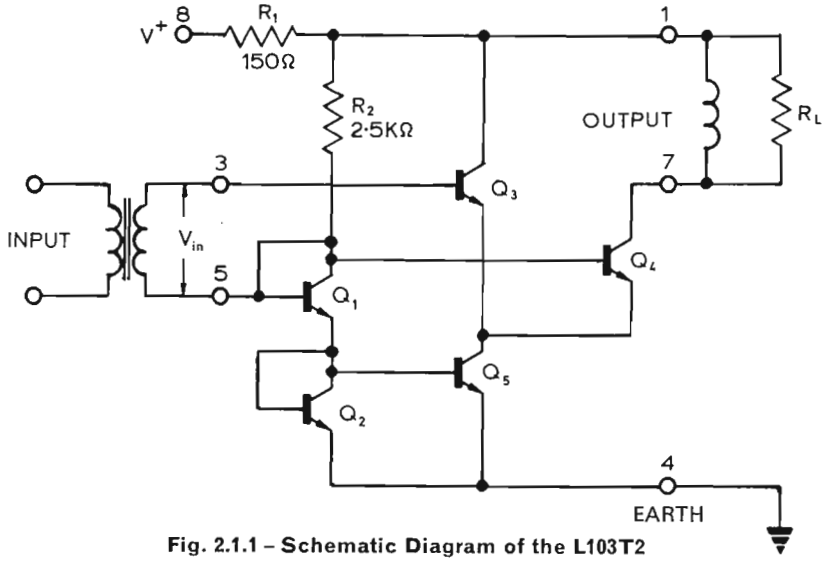


Fig. 2.1.1 – Schematic Diagram of the L103T2

The biasing arrangement takes advantage of the closely-matched characteristics of integrated circuit transistors, while the D.C. return path for biasing the input and output is provided by interstage transformer coupling. A single voltage supply is all that is required for operation.

The simplicity of the amplifier is demonstrated by the fact that it is constructed on a 20-mil square silicon chip (Figure 2.1.2) – a size which is small by comparison to many discrete transistors.

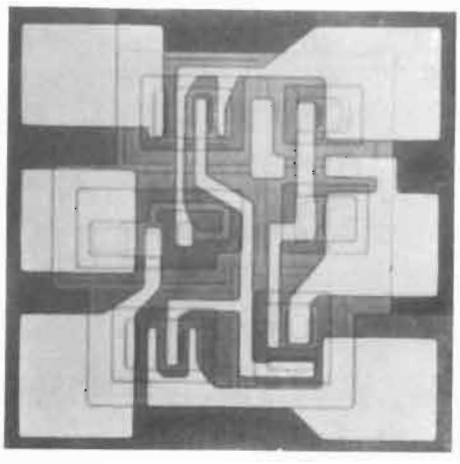


Fig. 2.1.2 – Photomicrograph of the L103T2

2.1.2 Circuit Description

The analysis of the L103T2 is simplified if the circuit is initially divided into a differential pair (Q_3 and Q_4) and its associated bias circuitry. Relationships may then be derived between the transfer function of the pair and its terminal currents and voltages.

The biasing is easily understood if it is assumed that all parts within the circuit are well matched and the transistor current gains are high enough that the base currents can be neglected. It is also assumed that the transformer windings, particularly in the input circuit, have a low enough D.C. resistance to be neglected.

The collector current of the biasing diode-connected transistor, Q_2, is

$$I_{C2} = \frac{V^+ - 2V_{BE}}{R_2 + 2R_1} \simeq \frac{V^+}{R_2}$$

since $R_2 >> R_1$ and $V^+ >> 2V_{BE}$.

All of the transistors are assumed to be identical; hence the collector current of Q_5 is equal to that of Q_2 because their bases are fed from a common voltage point. The collector current of Q_5 splits evenly between Q_3 and Q_4 with zero input signal. When the amplifier is driven into limiting, this current is alternately switched between Q_3 and Q_4. To prevent saturation of Q_4 when the amplifier is driven with a large signal, the load resistance must be low enough that current limiting occurs before the output voltage drops to $2V_{BE}$. Thus, for a transformer-coupled output.

$$R_L \leq \frac{2(V^+ - 2V_{BE})}{I_{C2}}$$

$$\leq 2R_2 \qquad \ldots\ldots\ldots (1)$$

For convenience in designing with the L103T2 in high-frequency IF and RF circuits, it is best characterised as an active two-port network with short-circuit admittance parameters used to describe its behaviour. Figure 2.1.3 shows the equivalent circuit for the amplifier, where the following y-parameters have been used:

input admittance	y_{11}
reverse transadmittance	y_{12}
forward transadmittance	y_{21}
output admittance	y_{22}

For frequencies low enough that reactive effects can be ignored, the forward transadmittance can be found with the aid of Equation (8) of section 2.1.2 in 'the application of linear microcircuits', Volume 1, which states that the difference in base-emitter voltage of two identical transistors as a function of their collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \left[\frac{I_2}{I_1}\right] \qquad \ldots\ldots\ldots (2)$$

From Equation (2) the relationship between the input voltage to the L103T2 and the collector currents in the differential pair is given by

$$V_{in} = \frac{kT}{q} \log_e \left[\frac{I_{C3}}{I_{C4}}\right] \qquad \ldots\ldots\ldots (3)$$

Since the sum of the collector currents of Q_3 and Q_4 is equal to the current source current (I_{C5}), Equation (3) may be expressed as

$$V_{in} = \frac{kT}{q} \log_e \left[\frac{I_{C5} - I_{C4}}{I_{C4}}\right] \qquad \ldots\ldots\ldots (4)$$

from which

$$I_{C4} = \frac{I_{C5}}{1 + \exp\left[\frac{qV_{in}}{kT}\right]} \qquad \ldots\ldots\ldots (5)$$

2.1.3 Circuit Performance

Equation (5) defines the transfer characteristic of the amplifier, and is plotted in Figure 2.1.4 for a typical device.

The forward transadmittance of the L103T2 may be obtained from Equation (5) according to the standard two-port parameter definition.

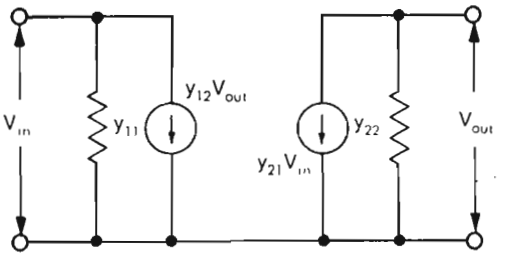


Fig. 2.1.3 – y Parameter Equivalent Circuit of the L103T2

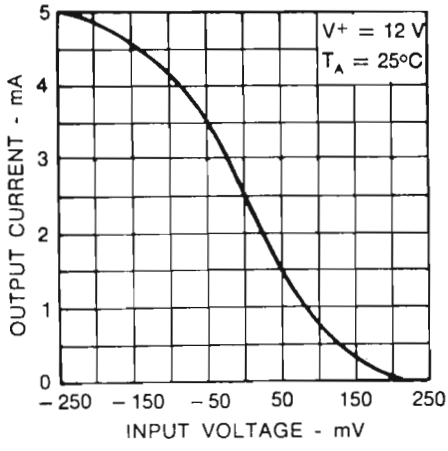


Fig. 2.1.4 – Transfer Characteristic of the L103T2

$$y_{21} = \frac{\delta I_{C4}}{\delta V_{in}}$$

$$= -\frac{qI_{C5}}{kT} \frac{\exp\left[\frac{qV_{in}}{kT}\right]}{\left[1 + \exp\frac{(qV_{in})}{kT}\right]^2}$$

$$= -\frac{q}{kT}\frac{I_{C5}}{2}\left[\frac{1}{1 + \cosh\left[\frac{qV_{in}}{kT}\right]}\right]$$

..... (6)

Figure 2.1.5 shows the forward transadmittance as a function of input voltage calculated from Equation (6). Note that y_{21} is maximum when the collector currents of Q_3 and Q_4 are equal to each other and equal to one-half the source current. A large resistance between the two input terminals can cause V_{in} to be different than zero because of the D.C. voltage drop across the resistance produced by the base current of Q_3. This results in a shift of the operating point of the y_{21} curve to somewhere below maximum. Therefore, low D.C. source impedance or transformer coupling should be used with the L103T2.

The effect of contact resistance in Q_3 and Q_4 has not been included in the analysis. By simple superposition, it can be shown that it merely decreases the maximum transadmittance available. The relative position of the maximum with respect to V_{in} is not altered. In addition, some desensitivity to input voltage will be realised because of emitter degeneration. This is also shown in Figure 2.1.5.

The input impedance is also a function of input voltage, increasing with large signals. This is because one transistor in the differential pair is being driven towards cutoff, which results in a

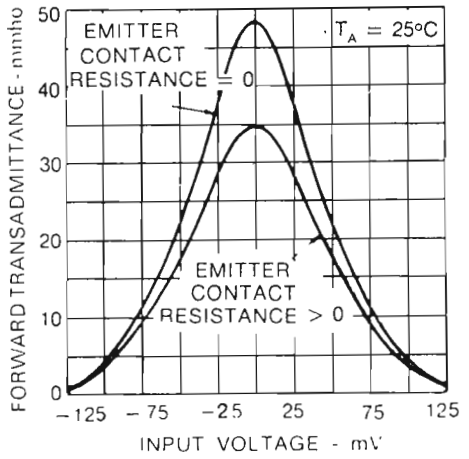


Fig. 2.1.5 – Forward Transadmittance as a Function of Input Voltage of the L103T2

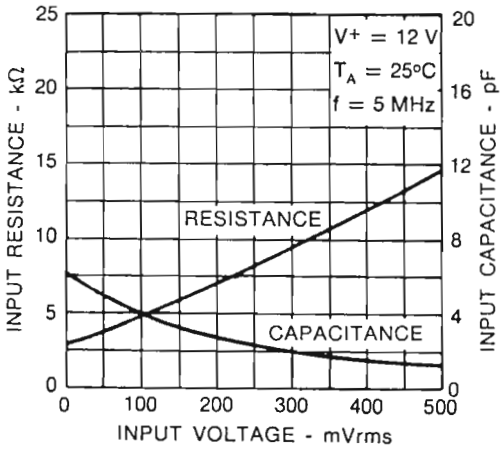


Fig. 2.1.6 – Input Resistance and Capacitance as a Function of Input Voltage of the L103T2

PARAMETER	CONDITIONS	VALUE	UNIT
	(T_A = 25°C, V^+ = 12 V unless otherwise specified)		
Power Consumption	$e_{in} = 0$	110	mW
Quiescent Output Current	$e_{in} = 0$	2.5	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	5	mA_{pp}
Output Saturation Voltage		1.4	V
Forward Transadmittance	e_{in} = 10 mV rms, f = 1 kHz	35	mmho
Reverse Transadmittance	f ≤ 5 MHz	0.001	mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz	0.3	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz	7	pF
Output Capacitance	f ≤ 5 MHz	2	pF
Output Conductance	f ≤ 5 MHz	0.02	mmho
Noise Figure	f = 30 MHz, R_S = 500Ω	6.5	dB
	f = 100 MHz, R_S = 500Ω	8	dB

Table 1

large emitter resistance. Figure 2.1.6 shows how both input resistance and capacitance vary with signal level.

Overall performance of the amplifier is summarised in Table 1.

The preceding analysis and figures were based on an operating temperature of 25°C and a frequency low enough that reactive terms could be neglected. If the effect of temperature is included, the output current will vary according to the matching and tracking of the transistor, and the change in resistor values. Figure 2.1.7 shows the transfer function for two temperature extremes, the stability of the quiescent operating point is given in Figure 2.1.8 and that of the forward transadmittance by Figure 2.1.9. The power consumption changes little with temperature, as illustrated in Figure 2.1.10. Additionally, quiescent operating conditions as a function of supply voltage are given in Figures 2.1.11 and 2.1.12.

Curves showing the frequency dependence of the two-port parameters of the L103T2 are given in Figures 2.1.13 to 2.1.15. As can be seen, there is little change from the low frequency values for frequencies less than 5–10 MHz. The frequency variation of the input, output and transfer admittance justify the equivalent circuit of Figure 2.1.3 and are typical of most two-ports.

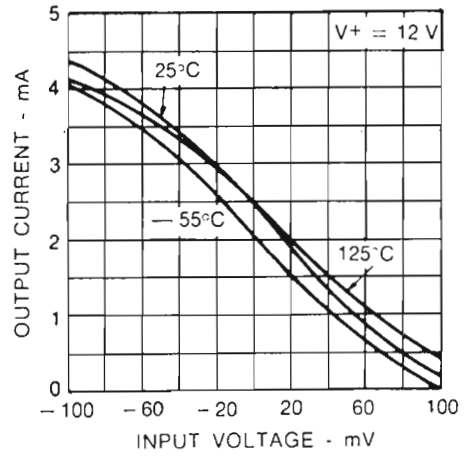


Fig. 2.1.7 – Transfer Characteristic as a Function of Temperature of the L103T2

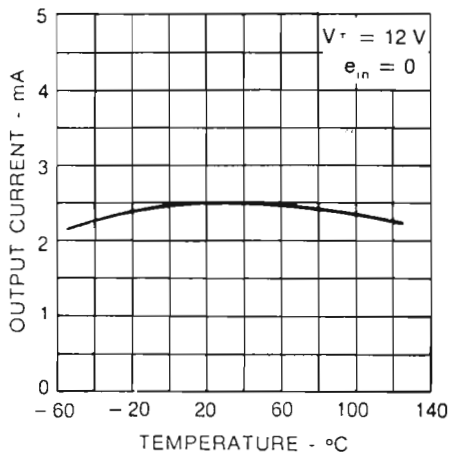


Fig. 2.1.8 – Output Current as a Function of Ambient Temperature of the L103T2

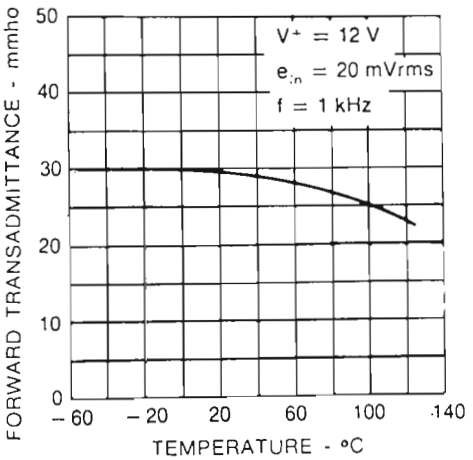


Fig. 2.1.9 – Forward Transadmittance as a Function of Ambient Temperature of the L103T2

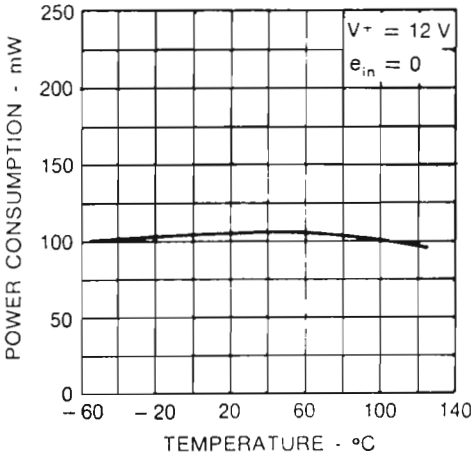


Fig. 2.1.10 – Power Consumption as a Function of Ambient Temperature of the L103T2

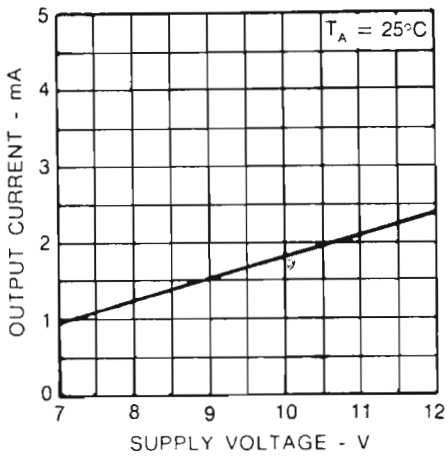


Fig. 2.1.11 – Output Current as a Function of Supply Voltage of the L103T2

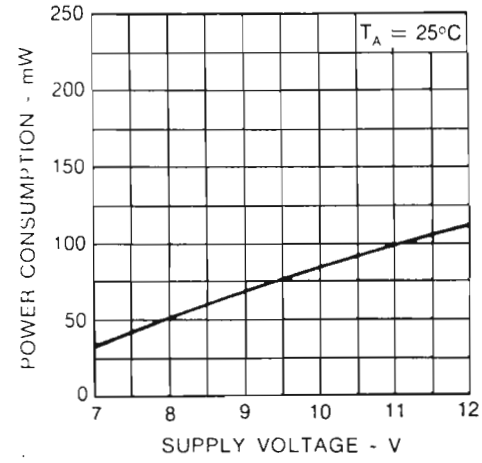


Fig. 2.1.12 – Power Consumption as a Function of Supply Voltage of the L103T2

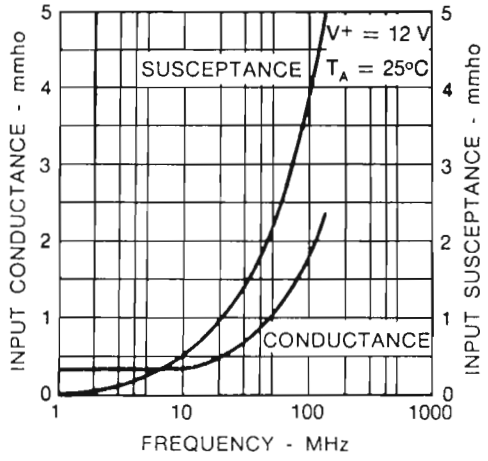


Fig. 2.1.13 – Input Admittance as a Function of Frequency of the L103T2

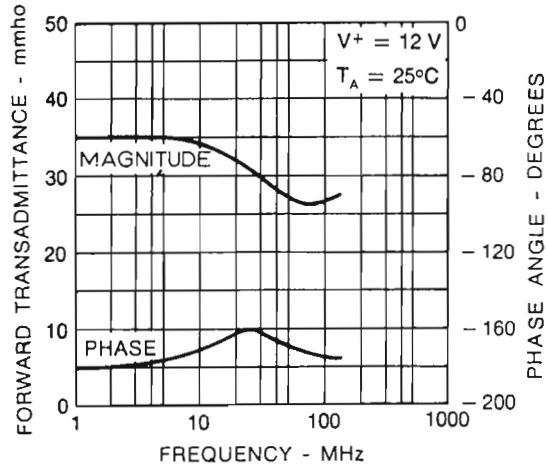


Fig. 2.1.14 – Forward Transadmittance as a Function of Frequency of the L103T2

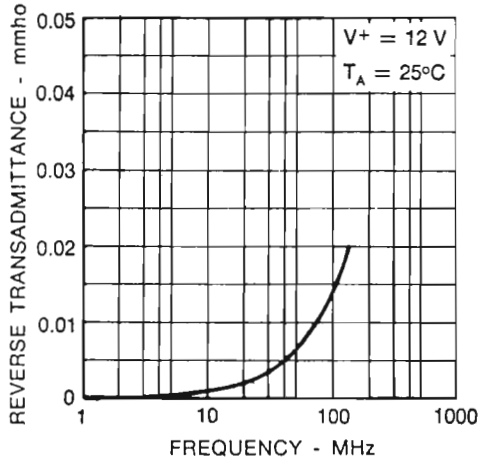


Fig. 2.1.15 – Maximum Reverse Transadmittance as a Function of Frequency of the L103T2

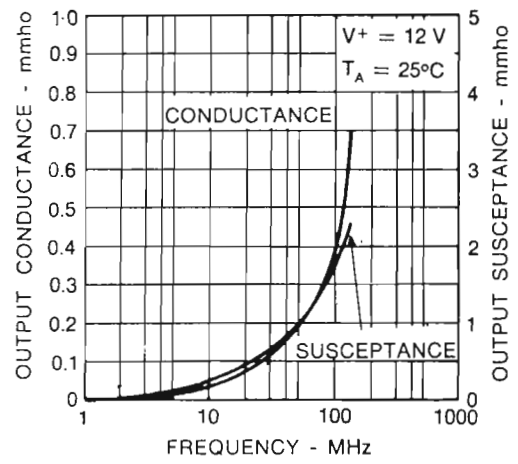


Fig. 2.1.16 – Output Admittance as a Function of Frequency of the L103T2

RF Amplifiers

Unneutralised small-signal amplifiers have a feedback path which can cause the real part of the input admittance of the device to become negative for certain combinations of frequency and load impedance. If this situation occurs, and the source admittance is equal to or less than the negative real part of the input admittance, self-sustaining oscillations are possible. For the typical amplifier, the designer has one of two choices: feedback that is equal in magnitude and opposite in phase to that inherent in his device can be applied around the circuit, or the interstage coupling networks can be loaded sufficiently to make the input admittance always greater than zero. These solutions have major drawbacks – neutralisation is at best a marginal solution since it is very frequency-sensitive and must be different for each situation. Loading the interstages is less frequency-sensitive, but the resultant mismatch loss is not always tolerable. The most satisfactory solution would be to use a device that possesses negligible intrinsic feedback – if an amplifier of that description does indeed exist. This ideal is closely approached by the L103T2, which has internal feedback an order of magnitude less than most high-frequency transistors. For example, a reverse transadmittance of less than 0.001 mmho at 10 MHz is not unusual.

The effect of input and output loading on the stability of the amplifier can best be seen from the expression for power gain of the device. The equivalent circuit of a typical RF amplifier, including source and load admittances, is shown in Figure 2.1.17. The expression for the input power (P_i) is

$$P_i = |V_1|^2 \, \mathrm{Re}\,(Y_{in})$$

$$= |V_1|^2 \, \mathrm{Re}\left[y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L}\right] \qquad \ldots\ldots\ldots (7)$$

and the output power is:

$$P_O = |V_2|^2 \, \mathrm{Re}\,(Y_L) \qquad \ldots\ldots\ldots (8)$$

From Figure 2.1.17,

$$|V_2| = \frac{|y_{21}|\,|V_1|}{|y_{22} + Y_L|} \qquad \ldots\ldots\ldots (9)$$

so

$$P_O = \frac{|y_{21}|^2 \mathrm{Re}\,(Y_L)}{|y_{22} + Y_L|^2} \; |V_1|^2 \qquad \ldots\ldots\ldots (10)$$

and the power gain becomes

$$\frac{P_O}{P_i} = \frac{|y_{21}|^2 \, R_e\,(Y_L)}{|y_{22} + Y_L|^2 \mathrm{Re}\left[y_{11} - \dfrac{y_{12}\, y_{21}}{y_{22} + Y_L}\right]} \qquad \ldots\ldots\ldots (11)$$

It can be seen from Equation (11) that the amplifier will be stable if

$$\mathrm{Re}\left[y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L}\right] > 0 \qquad \ldots\ldots\ldots (12)$$

Equation (12) can be manipulated to yield

$$2g_{11}\,(g_{22} + G_L) - \mathrm{Re}\,(y_{12}\, y_{21}) - |y_{12}\, y_{21}| > 0 \qquad \ldots\ldots\ldots (13)$$

where the 'g' terms represent the real parts of the admittance parameters.

If the power gain is reckoned from the terminals 'XX', Equation (13) becomes

$$2\,(g_{11} + G_S)\,(g_{22} + G_L) - \mathrm{Re}\,(y_{12}\, y_{21})$$

$$- |y_{12}\, y_{21}| > 0 \qquad \ldots\ldots\ldots (14)$$

Inspection of the above equation reveals that for unconditional stability at all frequencies, for any combination of source and load conductance, y_{12}, the reverse transadmittance, must equal zero. Since in practice y_{12} is finite, the source and load conductances must be manipulated to satisfy the stability criterion.

If it is assumed in Equation (13) that the real part of y_{12} is nearly zero, an expression can be obtained that will lead to a useful figure of merit for a two-port.

If $\mathrm{Re}\,(y_{12}\, y_{21})$ approaches zero, Equation (13) becomes

$$2g_{11}\,(g_{22} + G_L) - |y_{12}\, y_{21}| \geq 0 \qquad \ldots\ldots\ldots (15)$$

which for conjugate matching becomes

$$4g_{11}\, g_{22} \geq |y_{12}\, y_{21}| \qquad \ldots\ldots\ldots (16)$$

For conditional stability,

$$4g_{11}\, g_{22} = |y_{12}\, y_{21}| \qquad \ldots\ldots\ldots (17)$$

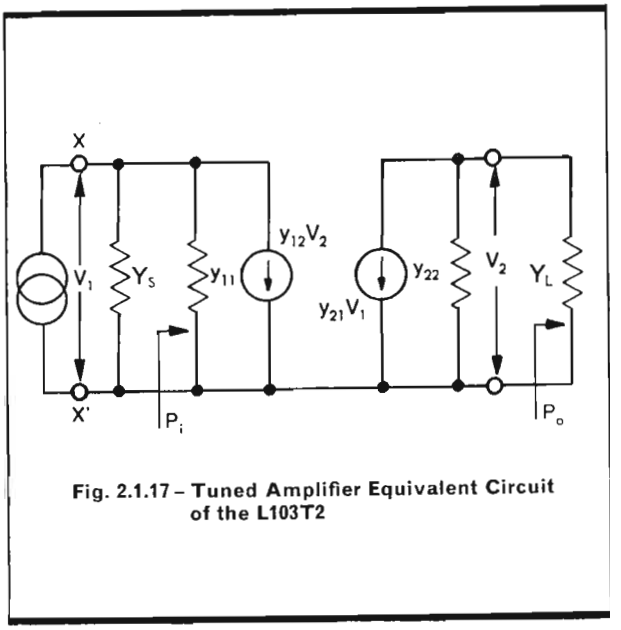


Fig. 2.1.17 – Tuned Amplifier Equivalent Circuit of the L103T2

The maximum gain that can be obtained from the two-port when the device is neutralised and conjugately matched is, from Equation (11),

$$\frac{P_o}{P_i} = \frac{|y_{21}|^2}{4g_{11}\,g_{22}} \qquad \ldots\ldots\ldots (18)$$

The maximum stable gain (a figure of merit for high-frequency transistors and amplifiers) is

$$GMS = \left|\frac{y_{21}}{y_{12}}\right| \qquad \ldots\ldots\ldots (19)$$

Obviously, the smaller y_{12} is, the greater will be the available stable gain. For very small values of y_{12}, the gain will be determined essentially by the input and output parameters of the device. For typical high frequency transistors at 10 MHz, the GMS is 27dB, while a GMS of 40dB can be obtained with the L103T2 at this frequency. Thus, fewer stages are required to achieve a given total gain.

A simplified design procedure for a 30 MHz amplifier that will serve to illustrate the practical aspects of the preceding discussion can now be presented. The first problem that must be considered is: 'How much gain can be realised at a given frequency?' To evaluate this problem, consider Equation (19) and the device parameters listed in Table 2 (taken from the curves of Figures 2.1.13 to 2.1.16). At 30 MHz, the forward transadmittance, y_{21}, is equal to 32 mmhos and the reverse transadmittance, y_{12}, is 0.004 mmhos. The maximum stable gain, GMS, is therefore 39dB.

PARAMETER	VALUE	UNIT
Input Resistance	1.7	kΩ
Input Capacitance	9	pF
Output Conductance	0.08	mmho
Output Capacitance	2.5	pF
Forward Transadmittance	32/140°	mmho
Reverse Transadmittance	0.004	mmho

Table 2

To obtain this gain, two conditions must be satisfied by the circuit. First, the source and load admittances have to be conjugately matched to the device, otherwise maximum transfer of power from source to load cannot be obtained. Second, the layout of the components must be such that feedback from output to input and from amplifier to external components is minimised.

The turns ratio of the input and output transformers are selected to provide a conjugate match to the device parameters listed in Table 2. The actual circuit details are shown in Figure 2.1.18 and the performance is listed in Table 3. Excellent agreement is seen to exist between measured and calculated power gain. Interaction between interstage coupling networks is minimal.

PARAMETER	VALUE	UNIT
Power Gain	35	dB
Bandwidth	1	MHz
Noise Figure	6	dB
Power Gain (calculated)	37.4	dB
Maximum Stable Gain	39	dB

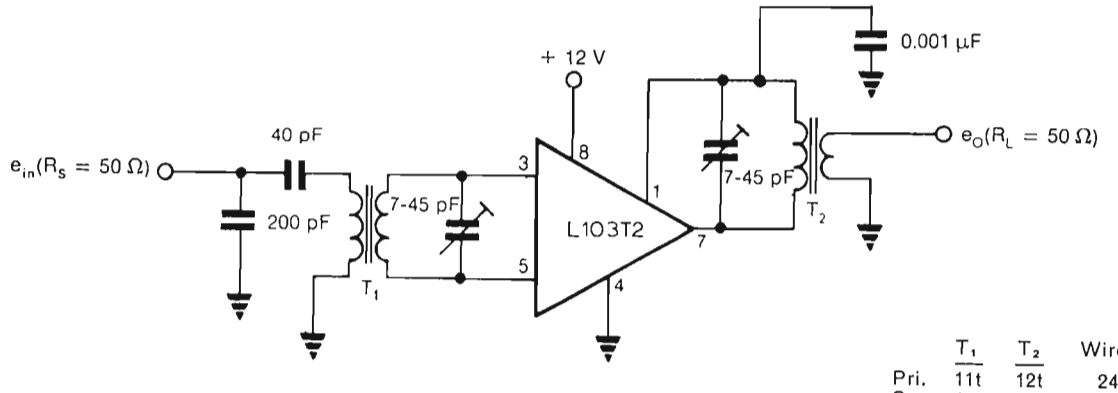
Table 3

Note that the amplifier does not utilise the limiting characteristic of the emitter-coupled pair and will saturate for large output swings. The input impedance does not drop, however, as the amplifier is driven into saturation.

Limiting RF Amplifiers

The preceding discussion of the small signal amplifier can be extended to limiting amplifiers without exception. The only additional requirement that must be fulfilled is that given by Equation (1) which ensures that the output transistor will not be saturated.

An amplifier which has a symmetrical output voltage limiting characteristic can be obtained from the circuit of Figure 2.1.18 by a minor modification in the output transformer. The effective turns ratio is adjusted so that the 50Ω load, in



	T_1	T_2	Wire size
Pri.	11t	12t	24 swg
Sec.	11t	1t	24 swg

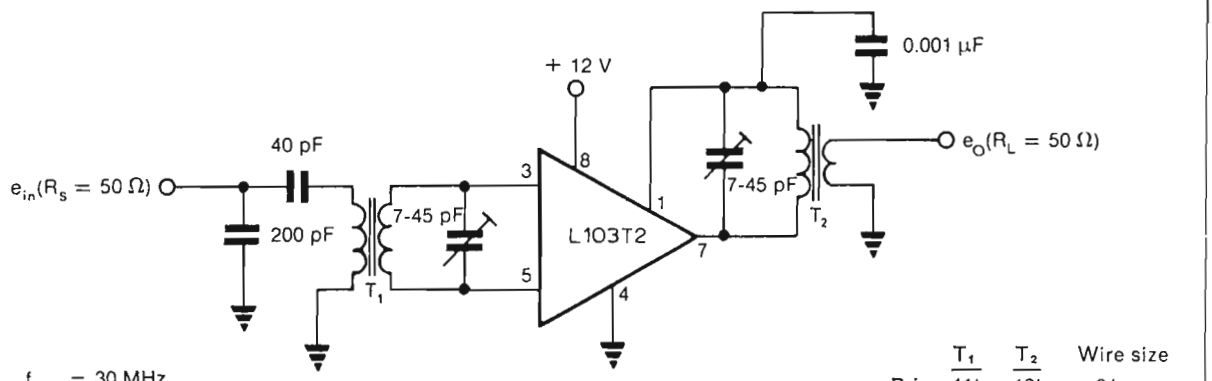
Transformer assemblies Neosid A7

Fig. 2.1.18 – 30 MHz RF Amplifier

parallel with the output resistance of the amplifier, causes the inequality of Equation (1) to be satisfied.

For the 12 V power supply and a 5 mA maximum collector current, the effective load should be less than 4.5 KΩ. Figure 2.1.19 shows the modified amplifier, designed for a 4.5 KΩ load and an output swing of $22V_{pp}$, with the measured performance characteristics.

Further examples of circuits using the L103T2 are given in the Applications section.



f = 30 MHz
BW = 1.6 MHz
PG = 30 dB
NF = 6 dB

	T_1	T_2	Wire size
Pri.	11t	12t	24 swg
Sec.	11t	3t	24 swg

Transformer assemblies Neosid A7

Fig. 2.1.19 – Limiting RF Amplifier

2.2 THE L123T2 VOLTAGE REGULATOR

2.2.1 Introduction

One of the commonest circuits in electronics is the voltage regulator. Virtually all circuits require a power supply and many of these must be stabilised. Many monolithic and hybrid voltage regulators suffer from the following disadvantages: poor accuracy, low output current and the inability to operate from high voltage or negative supplies. The L123T2 overcomes these disadvantages and in addition is competitively priced, when compared to discrete designs.

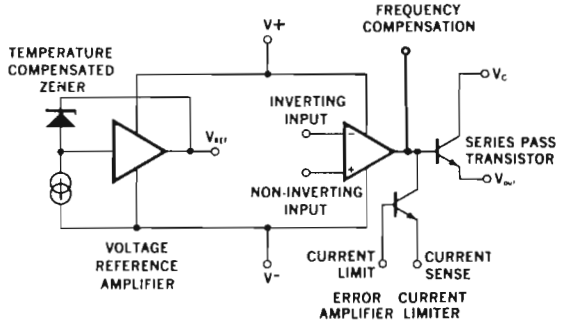


Fig. 2.2.1 – Equivalent Circuit of the L123T2

2.2.2 Circuit Description

Figure 2.2.1 shows the block diagram of the L123T2 from which can be seen the versatility of the device.

This is enhanced by the interconnection options which include the following:

(1) Internally generated reference voltage which is buffered and brought out for use in a variety of connections.
(2) Both inputs to the error amplifier are available to allow additional flexibility for negative supplies or high voltages.
(3) The collector of the internal power transistor is separated from the internal circuitry and is available separately.

Figure 2.2.2 shows the full circuit diagram of the L123T2.

The components Q_1, Q_2, D_1, R_1 and R_2 form the biasing network for the PNP current sources Q_3, Q_7 and Q_8. The N-channel FET (Q_1) is made with technology compatible with the production of standard integrated circuits. The use of an FET has two advantages. First, the line regulation is greatly improved because the current drawn by Q_1 is independent of power supply variations. Secondly, the power dissipation is minimised because the current drawn does not increase appreciably at large supply voltages. The diode D_1 helps to provide a well-regulated voltage at the base of Q_2 with respect to V^+.

The reference diode D_2 is contained in a feedback amplifier consisting of Q_4, Q_5 and Q_6, the constant current for Q_6 being provided by Q_3. By use of a feedback amplifier and the Darlington connection of Q_4 and Q_5 a reference voltage with a low output impedance is obtained. The necessary frequency compensation is provided by the MOS

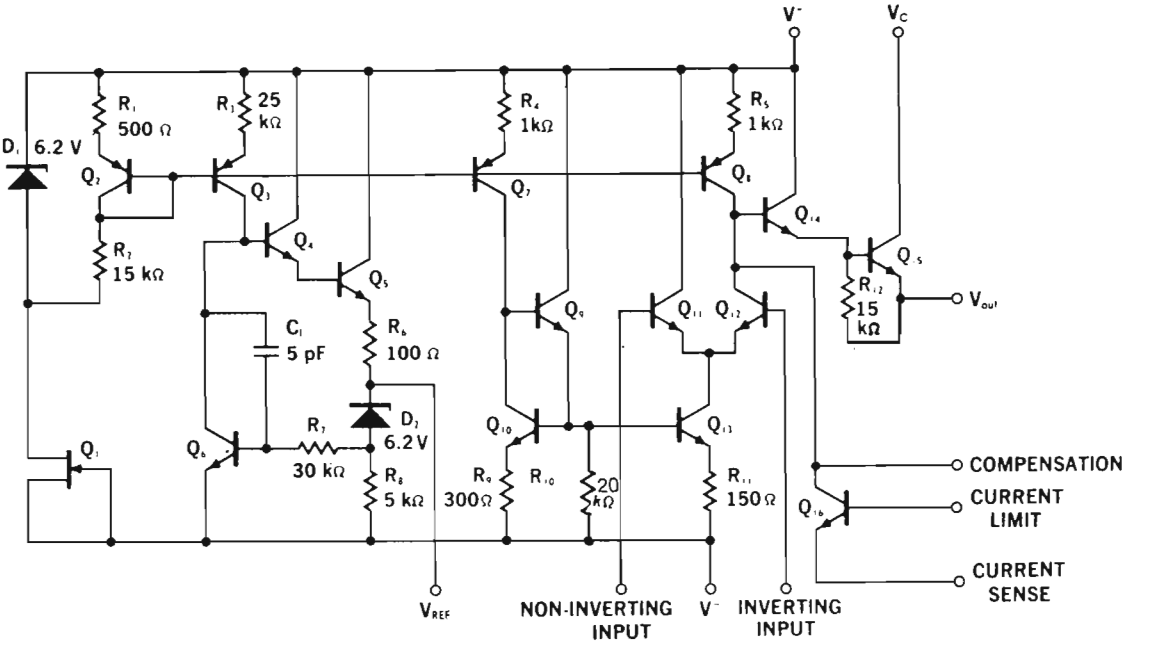


Fig. 2.2.2 – Circuit Diagram of the L123T2

capacitor C_1 (see section 2.4.2, Frequency Compensation).

The error amplifier is formed by the differential amplifier Q_{11} and Q_{12}. Using a current source (Q_8) instead of a resistor improves line and load regulation. A further improvement is obtained by using a current source in the tail of the differential amplifier. Frequency compensation can be achieved by connecting 100 pF between the compensation and inverting input pins or 1000 pF between compensation and earth. When external pass transistors are used these capacitors must be increased in value.

The power (series pass) transistor Q_{15} is a multiple device with individual emitter resistors to provide current sharing, increase the safe operating area and prevent secondary breakdown.

2.2.3 Circuit Performance

Details of electrical characteristics of the L123T1 and L123T2 are given on the respective data sheets. A brief summary of performance for a typical L123T2 is given below.

Line regulation (V_{in}=+12 to +15 V)	0.01% V_{out}
Load regulation (I_L=1 to 50 mA)	0.03% V_{out}
Ripple rejection	74 dB
Temperature coefficient of output voltage	0.003%/°C
Reference voltage	7.15 V
Output noise voltage	20μV
Long term stability	0.1%/1000 hours
Standby current drain (V_{in}=30 V)	2.3 mA
Output voltage range	2–37 V
Output current range	0–150 mA

As many different circuit configurations are available, reference should be made to the Applications section (3.2) for details of specific performance.

2.3 THE L127T2 TEMPERATURE CONTROLLED DIFFERENTIAL PREAMPLIFIER

2.3.1 Introduction

Many applications exist for very low drift amplifiers. Some of these are in the fields of low level transducers and high precision analogue computers. Existing linear integrated circuits, using closely matched bipolar input transistors in long tail pair configurations, allow drifts of 3 to 10μV/°C to be achieved. Where drift figures an order of magnitude lower are required several techniques have been used.

The most common technique is that of chopper stabilisation which can give excellent stability. Unfortunately the use of chopper amplifiers is limited by the following factors:

(1) Involved, time-consuming design and setting-up procedures.
(2) Size.
(3) Cost.
(4) Poor overload recovery.
(5) Undesirable shot noise.
(6) Poor reliability, owing to the large number of components used.

Another method is to mount the critical components inside an oven, held at a constant temperature. This has the disadvantages of high power consumption, increased size and weight together with reliability limitations.

A relatively new technique is the temperature stabilised chip which overcomes the disadvantages of the previous two methods. Here the chip of an integrated circuit is held at a constant temperature by an active regulator included on the chip. The chip is mounted within a high thermal resistance (500°C/Watt) TO–100 package to minimise the heater power and to ensure a rapid 'warm-up'. The possibility of integrating an entire operational amplifier on a temperature stabilised chip was examined. This was considered impractical because the changes in internal power dissipation (resulting from driving external loads) would require excessive power to be supplied to the regulator. Therefore a preamplifier was integrated into a temperature stabilised chip.

2.3.2 Circuit Description

Referring to Figure 2.3.1 the L127T2 is a two-stage differential input, differential output amplifier together with a temperature regulator.

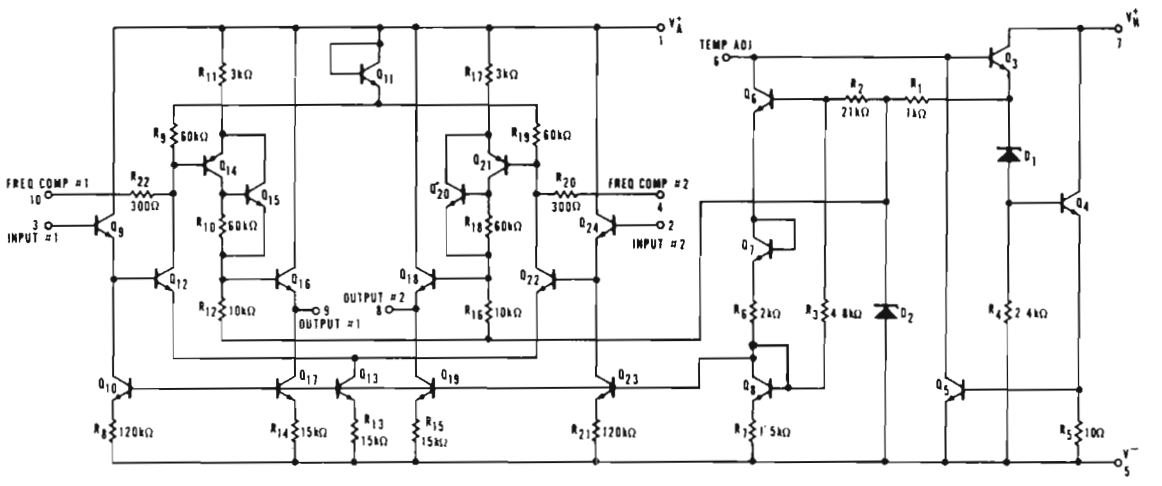


Fig. 2.3.1 – Circuit Diagram of the L127T2

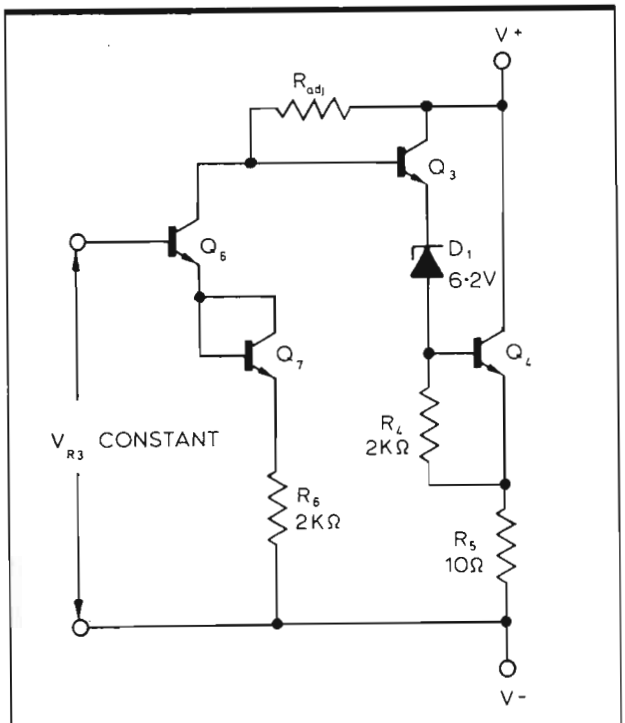


Fig. 2.3.2 – Simplified Circuit Diagram of the L127T2's Temperature Regulator

It is designed to drive existing integrated circuit amplifiers and comparators as well as discrete and hybrid amplifiers. The L127T2's voltage gain of 100 (typical) is sufficiently high to reduce the effects of drift in the following amplifier to negligible proportions, but is not high enough to make frequency compensation difficult when used with an operational amplifier.

A differential input pair of transistors is buffered by a pair of emitter followers to achieve a high input resistance (300 MΩ typical) and correspondingly low bias and offset currents. The second stage employs compound pairs of PNP and NPN transistors to provide level shifting and some additional gain without loading the first stage.

A simplified circuit diagram of the temperature regulator is shown in Figure 2.3.2. Q_4 is a large geometry transistor designed to evenly distribute the power dissipation across the chip. The transistor Q_3 supplies the base current for Q_4 through the level shifting zener diode D_1. Initial turn on current limiting is provided by R_5 and Q_5 (shown in the full regulator circuit Figure 2.3.1). The turn on current is limited to approximately 60 mA and the chip temperature stabilises very rapidly, usually to 1°C of the desired value in 1 second.

OFFSET VOLTAGE NULLING

As the typical values of input offset voltage and differential voltage gain are 2 mV and 100 respectively, the differential output voltage would be 2 mV×100=0.2 volts. For many applications this would be unacceptable, therefore a method of nulling the input offset voltage is required. Two methods exist, one using a relatively high value potentiometer (1 MΩ) and the other using a lower value potentiometer (10 KΩ). These are shown in Figures 2.3.3 and 2.3.4 respectively both using the frequency compensation pins. The components used must be low temperature coefficient types so as not to degrade the performance of the L127T2. (A T.C. of 50 ppm/°C can cause up to 0.25μV/°C effective input drift.)

The method shown in Figure 2.3.3 is suitable for use where the L127T2 is operating from single supplies and/or where ultimate component economy is required. Leads to the 1 MΩ potentiometer should be kept short to minimise pick up. The method shown in Figure 2.3.4 is suitable for use where the L127T2 is operating from dual symmetrical supplies and where the potentiometer (10 KΩ) is remote from the L127T2.

FREQUENCY COMPENSATION

In applications using a L127T2 driving an operational amplifier, the frequency response characteristics of both amplifiers must be examined if overall negative feedback is to be applied. The frequency compensation may be carried out at any suitable point within the loop, following the usual criteria.

The same two pins on the L127T2 that are used for input offset voltage nulling may be used for frequency compensating purposes as shown in Figure 2.3.5.

To assist in this, two 300Ω resistors have been diffused on the chip in series with each pin so as to eliminate the need for an external resistor in many applications. Figure 2.3.6 shows the frequency response of the L127T2 for various values of compensation components. The curves, together with the corresponding characteristics of the operational amplifier, may be used to obtain stable performance in any specific application.

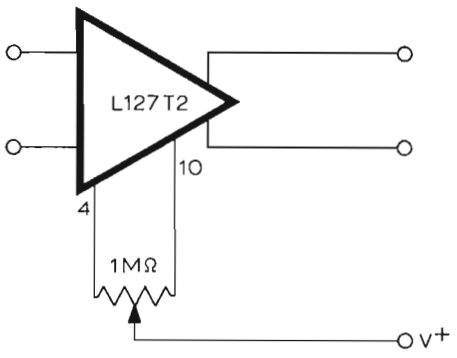


Fig. 2.3.3 – Offset Voltage Null Circuit

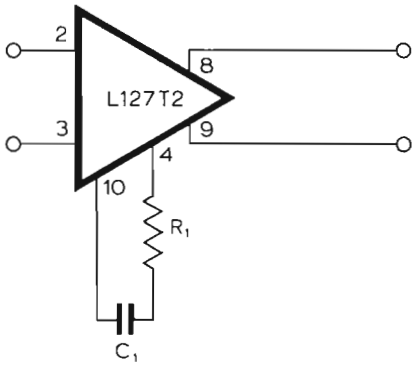


Fig. 2.3.5 – Frequency Compensation Circuit for the L127T2

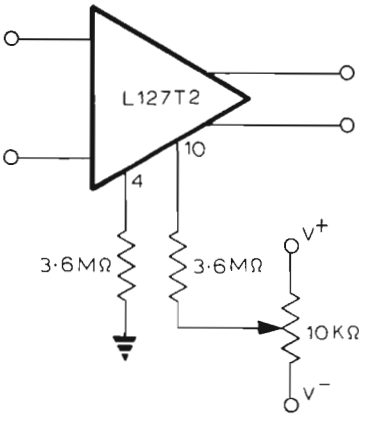


Fig. 2.3.4 – Offset Voltage Null Circuit

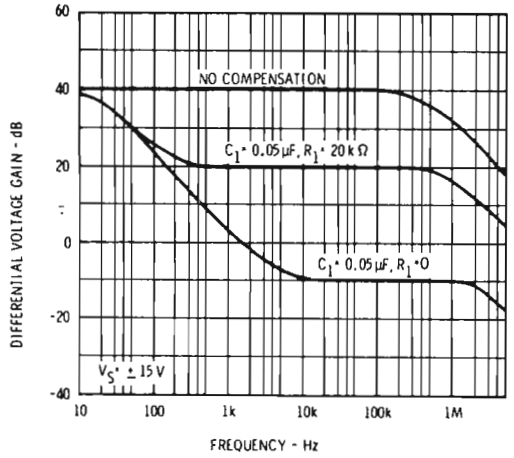


Fig. 2.3.6 – Open-loop Frequency Response for Various Values of Compensation Components

Input Offset Voltage		2 mV
Input Offset Current		2.5 nA
Input Bias Current		12 nA
Input Offset Voltage Drift	$-55 < T_A < 125°C$	0.6 µV/°C
Input Offset Current Drift	$-55 < T_A < 125°C$	2 pA/°C
Differential Input Resistance		300 MΩ
Common Mode Input Resistance		1000 MΩ
Input Voltage Range		±13 V
Output Common Mode Voltage		−5 V
Differential Output Voltage Swing		±7 V
Common Mode Rejection Ratio		100 dB
Supply Voltage Rejection Ratio		80 µV/V
Long Term Drift		5 µV/week
Differential Voltage Gain		100

2.3.3 Circuit Performance

Details of the electrical characteristics for the L127T2 and L127T5 are given on the respective Data Sheets. A brief summary of performance for a typical L127T2 is given above.

Conditions: $V_S = \pm 15$ V, $T_{AMB} = +25°C$

From this the superiority of the L127T2 over non-stabilised bipolar input stages is obvious. Figure 2.3.7 gives a comparison between the L127T2 and an FET input stage amplifier. This shows that the L127T2 has a superior drift performance for source resistances below 5 MΩ and for any source resistance when the ambient temperature is above +45°C (owing to the exponential behaviour of the FET's leakage current). Due to the temperature stabilisation there is virtually no change in any of the electrical characteristics over the full military temperature range, with the exception of the power dissipation which is inversely proportional to temperature as shown in Figure 2.3.8.

The versatility of the L127T2 is enhanced by the capability of operating over a supply voltage range of ±9 volts to ±18 volts with little degradation in performance. It is necessary to change the value of R_{adj} to maintain a constant substrate temperature. Figure 2.3.9 shows the values of R_{adj} for various values of supply voltage and for operation up to ambient temperatures of +70°C, +85°C or +125°C. The supplies to the device need not be symmetrical provided the total voltage applied is between 18 and 36 volts. As the output common mode voltage tracks the negative supply voltage the L127T2 can be used to drive amplifiers with a limited input common mode voltage, such as the µA702.

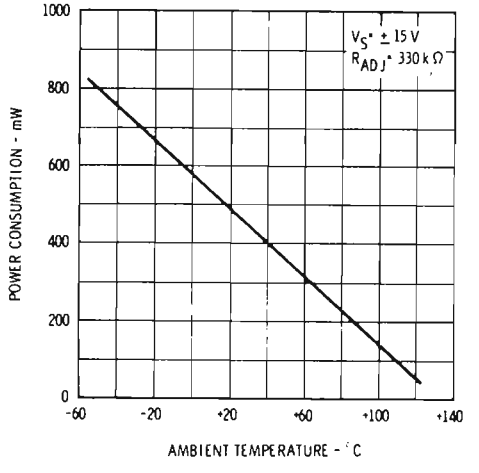


Fig. 2.3.8 – Power Consumption as a Function of Ambient Temperature of the L127T2

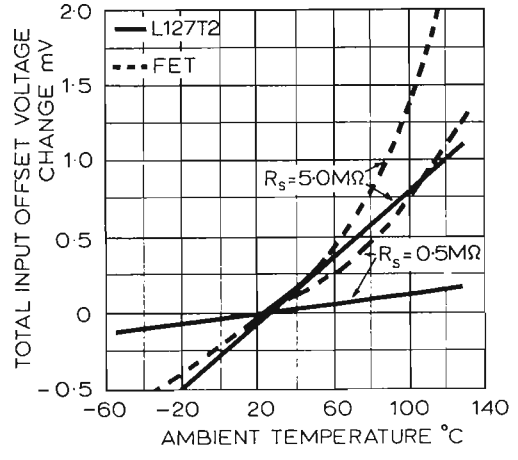


Fig. 2.3.7 – Performance Comparison of the L127T2 and an FET Input Stage Amplifier

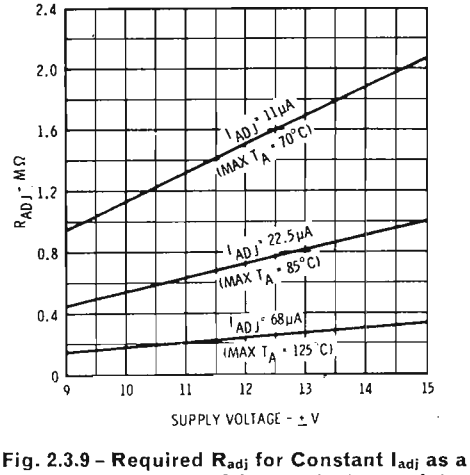


Fig. 2.3.9 – Required R_{adj} for Constant I_{adj} as a Function of Supply Voltage of the L127T2

2.4 THE L141T2 HIGH PERFORMANCE OPERATIONAL AMPLIFIER

2.4.1 Introduction

The L141T2 is a monolithic, linear integrated circuit constructed on a single silicon chip using the planar epitaxial process. It is pin compatible with the popular μA709 operational amplifier but has the following advantages:

(1) Output short circuit protected.
(2) Inputs latch-up proof.
(3) Large differential input voltage range (±30 V maximum).
(4) Internal frequency compensation.
(5) Simple input offset voltage nulling with one 10KΩ potentiometer.
(6) Wide operating voltage range (±3 V to ±20 V).
(7) Low power consumption.

The internal frequency compensation ensures stability of the amplifier for any value of closed loop gain down to unity. This reduces design, component costs, size/weight and increases reliability as no external components are required. The design of the output stage is such that oscillations will not occur when the amplifier is driving small value capacitive loads. In addition a class AB output stage is used, eliminating the crossover seen with earlier amplifiers.

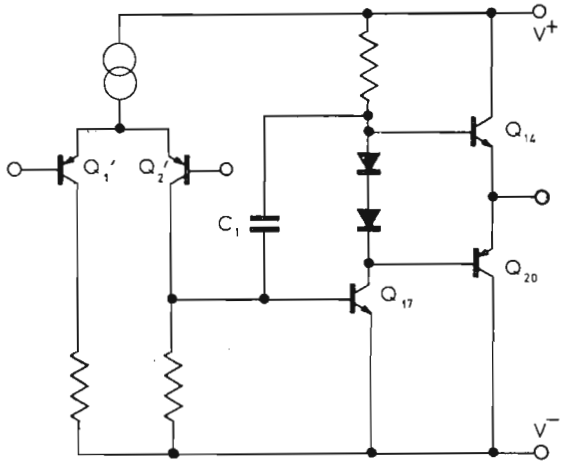


Fig. 2.4.1 – Simplified Circuit Diagram of the L141T2

2.4.2 Circuit Description

The circuit of the L141T2 is shown in much simplified form in Figure 2.4.1.

From this it can be seen that the amplifier consists of a high gain, differential input stage following by a high gain driver, feeding a class AB output stage. The full circuit diagram of the L141T2 is shown in Figure 2.4.2.

As the production of high h_{FE} PNP transistors involves costly additional processing steps in an integrated circuit, the input stage uses a combination of low h_{FE} PNPs and high h_{FE} NPNs to obtain small input bias currents. A particular ad-

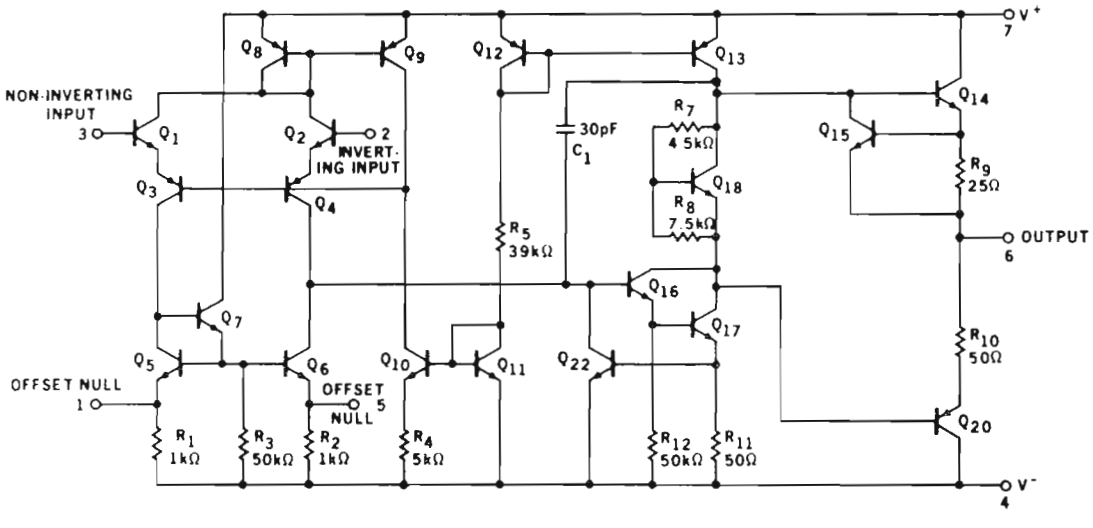


Fig. 2.4.2 – Circuit Diagram of the L141T2

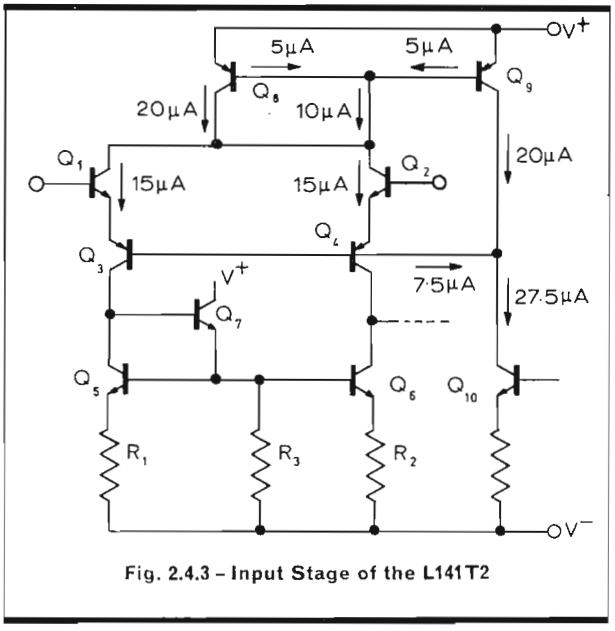


Fig. 2.4.3 – Input Stage of the L141T2

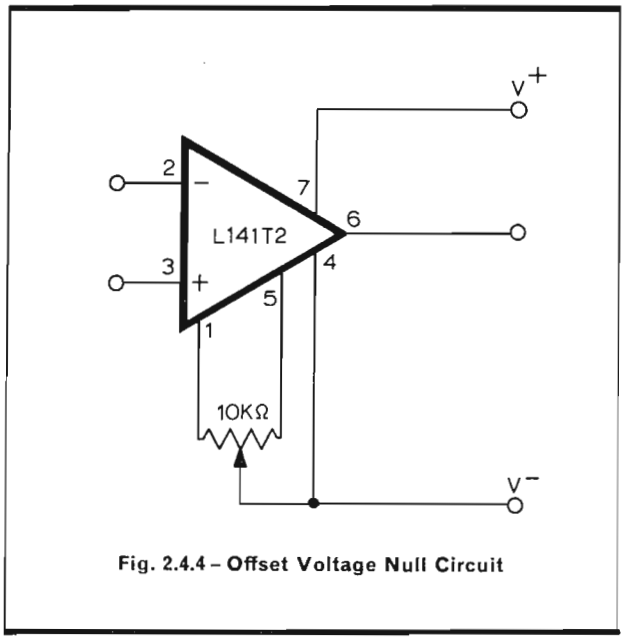


Fig. 2.4.4 – Offset Voltage Null Circuit

vantage of using this configuration (compared with the μA709) is its ability to withstand ±30 V differential input signals without breaking down the base/emitter junction of Q_1 or Q_2. This is due to the very much higher reverse base/emitter breakdown voltage (BV_{EBO}) of a lateral PNP transistor than that of an NPN transistor.

To achieve a high differential voltage gain from the input stage, the output resistances of Q_5 and Q_6 are used as loads, giving effective values of about 2MΩ. The high values of collector load resistance for the input stage are necessary because of the low collector currents used to obtain low input bias currents. These collector currents are defined by the bias network formed by the current source Q_{10} and the PNP transistors Q_8 and Q_9. The current levels under typical operating conditions are given in Figure 2.4.3.

The bias currents of Q_1 and Q_2 remain fairly constant for wide variations in the lateral PNP transistors and the technique does not require close h_{FE} matching.

The driver stage of the amplifier utilises a Darlington connection to prevent loading of the input stage. A conventional complementary symmetry class AB output stage is used. The quiescent current of approximately 60μA through the output transistors Q_{14} and Q_{20} eliminates the crossover distortion seen in many class B output stages.

The output stage incorporates current limiting circuitry to prevent excessive chip dissipation under short circuit conditions. For positive output currents this is achieved by Q_{15} and R_9. If the output current exceeds approximately 25 mA (at T_A=+25°C) the voltage drop across R_9 will cause Q_{15} to conduct. The output current will then be limited to about 25 mA. For negative output currents the limiting is achieved by R_{10} and the voltage drop across R_{11} causing conduction of Q_{22}. The amplifier is therefore able to withstand indefinite short circuits to earth or either supply rail. Since the maximum allowable dissipation decreases as the ambient temperature increases the current limiting has been designed to come in at a lower value of current at high temperatures, e.g. the short circuit current at an ambient temperature of +125°C is only ±17 mA (approximately) compared to ±25 mA (approximately) at +25°C. (Because of power dissipation limitations the protection is only valid up to ambient temperatures of +75°C).

Offset Voltage Nulling

In applications where nulling of the input offset voltage is required a 10KΩ potentiometer may be connected as shown in Figure 2.4.4.

This enables a variation of approximately ±25 mV referred to the input to be achieved. It would also be possible to adjust the offset voltage by using the collectors of Q_5 and Q_6. This method was not used on the L141T2 for two reasons. First, the very high value of potentiometer required (around 5MΩ) is not readily available in the popular 'trim-pot' form. Secondly, any external leads attached to these high impedance nodes may introduce stray pick-up into the amplifier.

Frequency Compensation

As stated in the introduction, the L141T2 does not require any external frequency compensation components, even for closed loop gains down to unity. The amplifier has an internal 20 dB/decade (6 dB/octave) roll off commencing at 10 Hz and passing through unity gain at 800 kHz. This ensures a phase margin at unity gain of 80° (typical).

The roll off is achieved with a 30 pF MOS capacitor diffused into the same silicon substrate as the amplifier. The presence of an MOS capacitor on the chip represents a significant advance in linear integrated circuit processing. The diffusion sequence used is no different in principle to that for comparable 40 V circuits but the fabrication of stable, close tolerance capacitors necessitates sophisticated and ultra-clean production techniques. The capacitor is formed between the n+ region and the larger of the two metallised layers using an oxide for the dielectric, as shown in Figure 2.4.5.

The built-in monolithic capacitor results in increased reliability, smaller circuit boards and lower assembly costs, as well as reducing the chances of an engineering error. Information of the frequency and phase response of the amplifier is given in Figure 2.4.6.

In applications where a reduced gain/bandwidth product is required an additional capacitor may be connected between pins 5 and 6.

2.4.3 Circuit Performance

The electrical parameters of the L141T2 are equal to or better than those of the μA709, with the exception of bandwidth and slewing rate, these being limited by the internal fixed frequency compensation. In addition the amplifier operates over a wider range of supply voltages (±3 V to ±20 V) and has a large input voltage range.

Typical performance figures for the L141T2 are summarised in Table 1. Figure 2.4.7 shows the change of open loop voltage gain with change of supply voltage to be very good. The low power consumption of the device is shown in Figure 2.4.8 for various values of supply voltage.

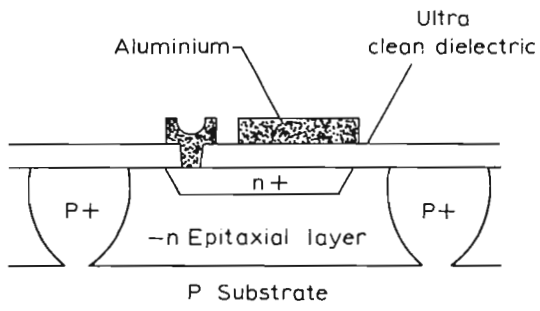


Fig. 2.4.5 – Construction of an MOS Capacitor

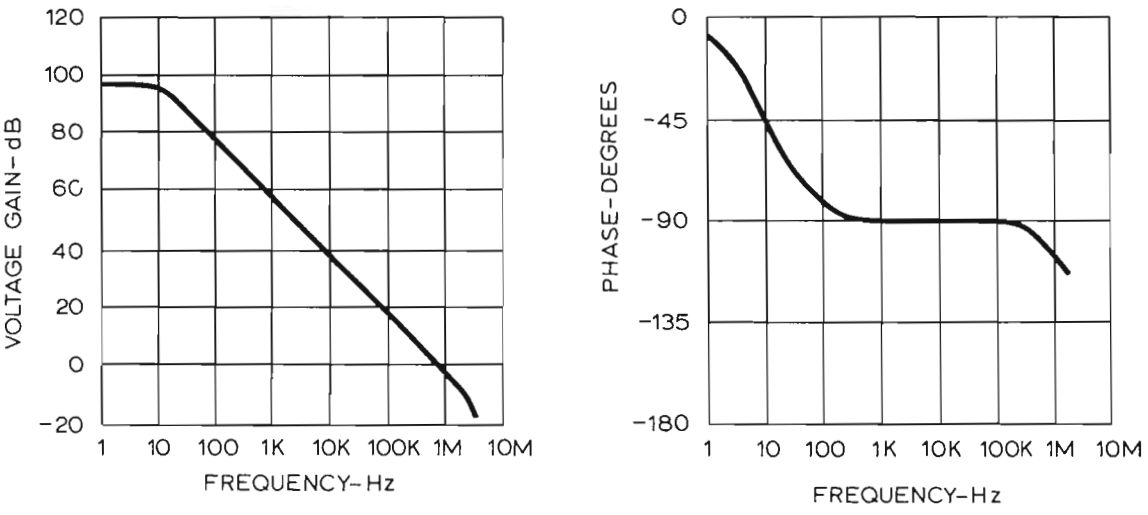


Fig. 2.4.6 – Frequency and Phase Response of the L141T2

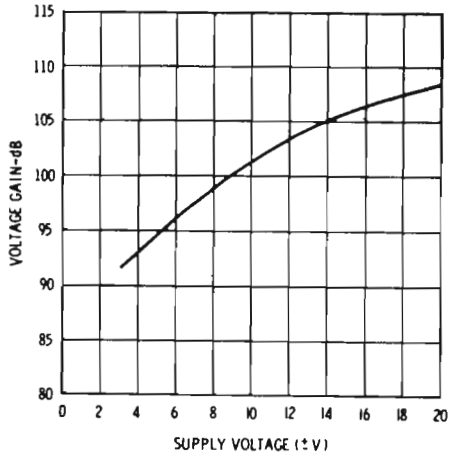


Fig. 2.4.7 – Open Loop Voltage Gain of the L141T2

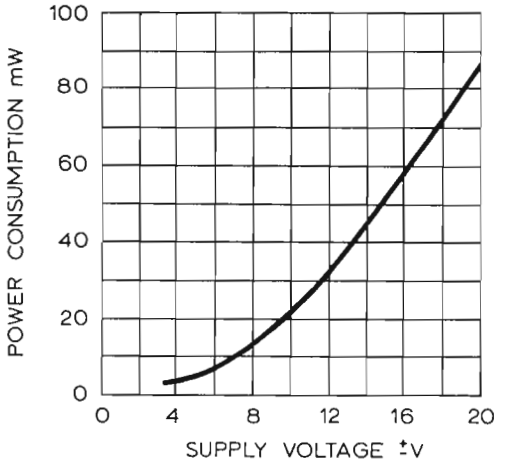


Fig. 2.4.8 – Power Consumption of the L141T2

PARAMETER	CONDITIONS	VALUE	UNITS
	($T_A = +25°C$, $V_S = \pm 15$ V)		
Input Offset Voltage	$R_S \leq 10\,k\Omega$	1.0	mV
Input Offset Current		30	nA
Input Bias Current		200	nA
Input Resistance		1000	kΩ
Large Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{OUT} = \pm 10$ V	200,000	
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±14	V
	$R_L \geq 2\,k\Omega$	±13	V
Input Voltage Range		±13	V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	90	dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$	30	µV/V
Power Consumption		50	mW
Transient Response (unity gain)	$V_{IN} = 20$ mV, $R_L = 2\,k\Omega$ $C_L \leq 100$ pF		
Risetime		0.3	µSec
Overshoot		5.0	%
Slew Rate (unity gain)	$R_L \geq 2\,k\Omega$	0.5	V/µSec

Table 1

3. LINEAR INTEGRATED CIRCUIT APPLICATIONS

3.1 L103T2 Basic Circuits

3.1.1 100 MHz and 200 MHz RF Amplifiers

Figure 3.1.1 shows the schematic of a 100 MHz RF amplifier using the L103T2. As with all circuits using the L103T2 at frequencies above 30 MHz, the low input terminal (pin 5) should be decoupled to earth. This is necessary for two reasons:

(1) The two diodes (or saturated transistors) between pins 5 and 4 are not a perfect short circuit and so do not completely decouple the base of the grounded base transistor of the emitter-coupled pair.

(2) The high frequency current gain is falling off at 6 dB/octave at frequencies above 30 MHz. This results in more base current at high frequencies and consequently more RF current in the two decoupling diodes or external decoupling capacitance.

Without the additional bypass capacitance, both the power gain and the gain figure are decreased by about 8 dB.

Typical Performance Figures
(12 V supply, f=100 MHz)

1. Power Gain 20–21 dB
2. Noise Figure 6 dB
3. Bandwidth 5 MHz
4. Maximum Stable Gain $\left|\frac{y_{21}}{y_{12}}\right| = 31$ dB

The y parameters for the L103T2 at 100 MHz are:

$y_{22} = 0.2+j1.5$ mmhos
$y_{11} = 1.2+j3$ mmhos
$y_{21} = 19$ mmhos
$y_{12} = 0.015$ mmhos

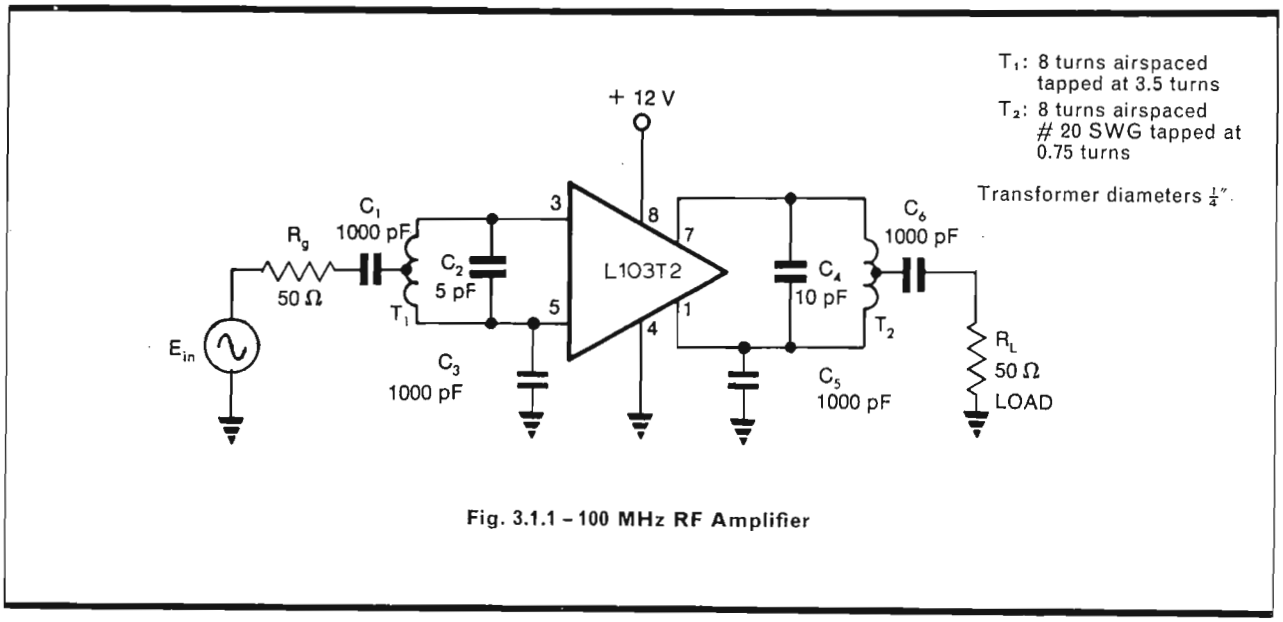


Fig. 3.1.1 – 100 MHz RF Amplifier

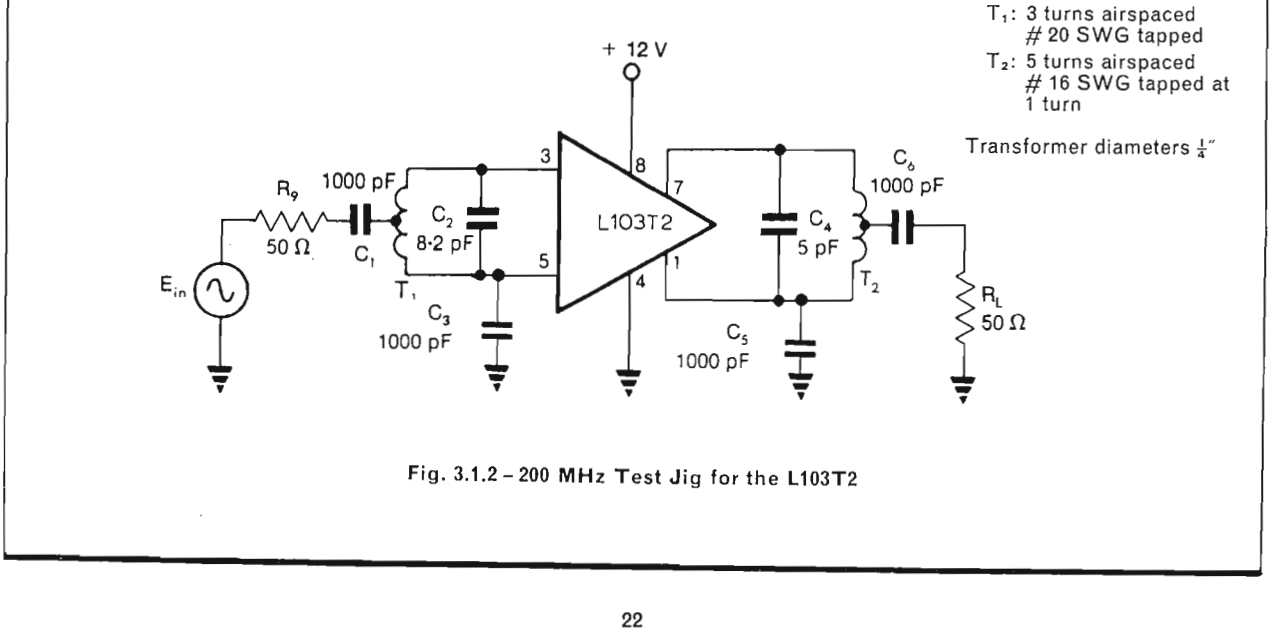


Fig. 3.1.2 – 200 MHz Test Jig for the L103T2

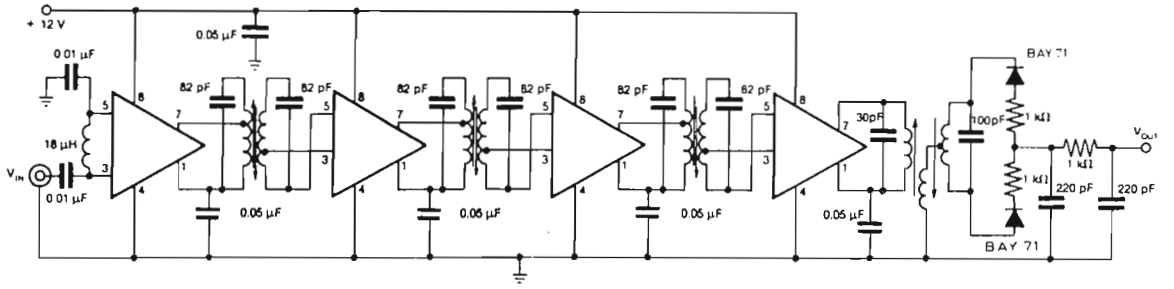


Fig. 3.1.3 – FM IF Amplifier using L103T2s

The L103T2 may be used as a current mode limiter if the total output admittance (including 'g_{22}') is more than about 0.3 mmhos. The power gain will be a little under 20 dB. Reverse AGC may be obtained by bleeding current from pin 5, thereby reducing the value of the current in the emitter-coupled pair.

The circuit for the measurement of power gain and noise figure at 200 MHz (Figure 3.1.2) is essentially the same as that used at 100 MHz with, of course, changes in the values of the tuning components.

Typical Performance Figures
(12 V supply, f=200 MHz)

1.	Power Gain	14 dB
2.	Noise Figure	7.5 dB
3.	Bandwidth (−3 dB)	10 MHz
4.	Maximum Stable Gain	20.5 dB

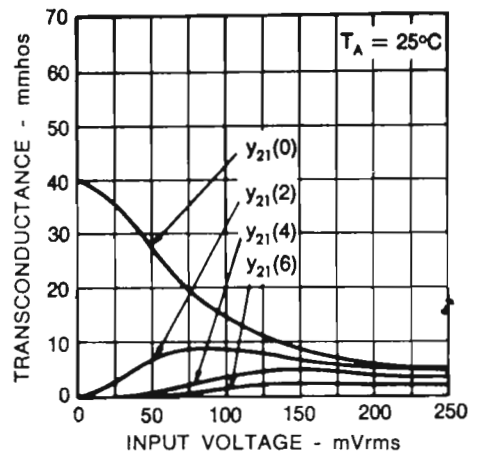


Fig. 3.1.4 – Forward Transconductance of Emitter-Coupled Pair for Even-Order Harmonics

The y parameters for the L103T2 at 200 MHz are:

y_{11} = 2+j6.3 mmhos
y_{22} = 0.7+j3.2 mmhos
y_{21} = 12 mmhos
y_{12} = 0.12 mmhos

3.1.2 FM IF Amplifier

The excellent limiting characteristics of the L103T2 make it particularly suitable for 10.7 MHz IF strips. Figure 3.1.3 shows the use of four L103T2s in a high quality FM tuner. Typical performance characteristics are:

Full limiting	50µV
Power gain per stage	26.5 dB
Peak-to-Peak separation of detector	800 kHz
THD (±75 kHz deviation at 400 Hz)	<0.8%
Current consumption	27 mA

3.1.3 Harmonic Mixer

The small-signal forward admittance of the L103T2 with a time-varying input signal is given by

$$y_{21}(t) = -\frac{q}{kT}\,\frac{I_{C5}}{2}\left[\frac{1}{1+\cosh\dfrac{qV_{in(t)}}{kT}}\right] \quad \ldots\ldots\ldots (1)$$

where:

$V_{in(t)}$ = $V_{lo}\cos\omega_{lo}t + V_S\cos\omega_s t$
V_{lo} = local oscillator voltage
ω_{lo} = local oscillator frequency
V_S = signal voltage
ω_s = signal frequency

For a harmonic mixer, the amplitude of the signal must be less than the local oscillator so that trans-admittance modulation of the L103T2 is accomplished essentially by V_{lo}.

Since the cosh function of Equation (1) is an even function, only components which are even multiples of the local oscillator frequency will be present in the output of the L103T2. The graphical solution of Equation (1) is shown in Figure 3.1.4 for the first three harmonics.

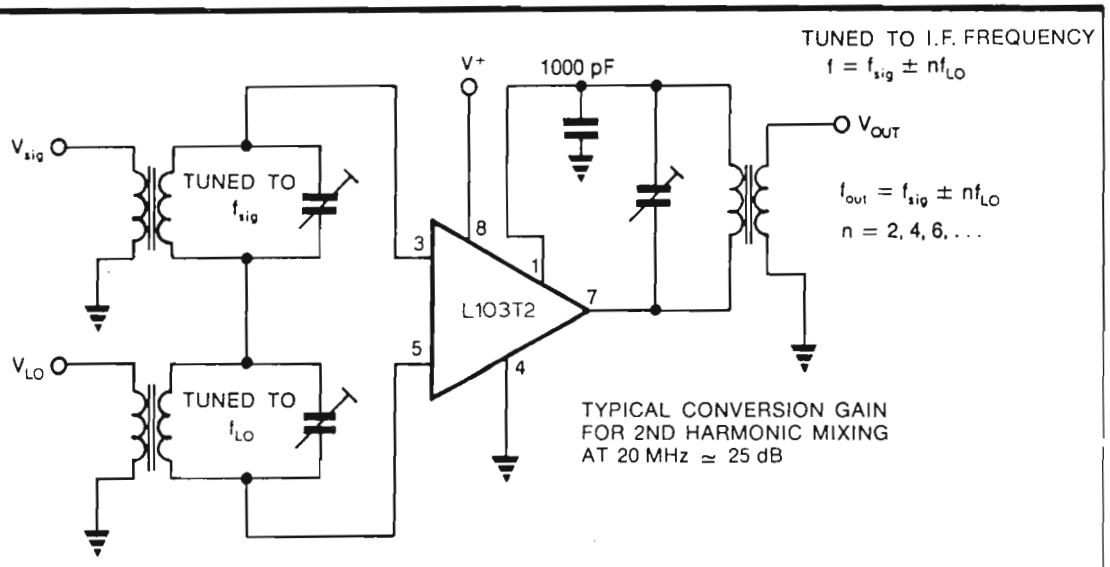


Fig. 3.1.5 – L103T2 Mixer Connection

A general algebraic solution is not attempted here since it would provide little more than exercise. It can be seen from the figure that the large local oscillator drive generates components of the forward transadmittance which are even functions only. This 'harmonic mixing' is more useful than a conventional mixer because of the lower frequencies and reduced filtering required. It would be much easier to design a 50 MHz oscillator than a 100 MHz oscillator for use as a local oscillator, for example. One possible configuration for the mixer is shown in Figure 3.1.5.

3.1.4 10 MHz Oscillator

The design of transistor oscillators is complicated by the loading of the tank circuit caused by the decrease in input impedance under large signal conditions. The usual solution is to provide some sort of impedance isolation between input and output, such as high turns ratio transformers or emitter-followers in the feedback loop.

The input impedance of the L103T2, however, tends to increase with large-signal inputs. This simplifies the oscillator design because the effect of input parameter variations can be neglected (this depends upon the input voltage swing, becoming more varied for larger signals, but is usually permissible for effective loads of 2 KΩ or less).

Predictable oscillator performance can be obtained by utilising the Barkhausen criterion for oscillations, which states that the necessary and sufficient condition for oscillations to occur is:

$$1 - GH = 0 \qquad \ldots\ldots\ldots (1)$$

where GH is the loop gain of the system, G is the forward transfer function, and H is the reverse (feedback) transfer function.

Assuming that the input admittance is small compared to the load admittance, and the oscillator frequency is less than the corner frequency of the forward transadmittance, the forward transfer function is given by

$$G = \frac{V_{OUT}}{V_{IN}}$$

$$= \frac{y_{21}}{g}\left[\frac{1}{1 - j\dfrac{1}{g\omega L}\left[1 - \dfrac{\omega^2}{\omega_o^2}\right]}\right] \qquad \ldots\ldots\ldots (2)$$

where:

$$\omega_o^2 = \frac{1}{LC}$$

C = load capacitance plus amplifier output capacitance

g = load conductance plus amplifier output conductance

Using a feedback transformer with a 1:1 turns ratio, and assuming that the coefficient of coupling is unity (which is usually justified if a toroidal core is used), the reverse transfer function H, will be equal to one. Therefore, for oscillations to occur at $\omega = \omega_o$, the load conductance must be small enough such that

$$\frac{y_{21}}{g} = \geq 1 \qquad \ldots\ldots\ldots (3)$$

The effect of the phase shift contributed by the high frequency pole of y_{21} is to reduce the actual frequency of oscillation, but since in most tuned oscillators a trimmer is used to set the final frequency, a more exact analysis is not justified. The effect of variations in input parameters was assumed negligible in the preceding discussions, any exact analysis, however, must account for

them as well as the transformer coupling co-efficient and losses.

The magnitude of the output voltage can be predicted quite well if the total voltage swing at the output collector of the device is allowed to be no more than 5 V_{pp} (for a 1:1 transformer, the maximum input voltage rating of the device will otherwise be exceeded and the emitter-base junctions may be damaged). Further, the effective collector load resistor must be small enough to ensure that current limiting occurs, but large enough that oscillations are maintained. The value of the load resistor can be determined from the expression

$$R_L = \frac{V_{pp}\,(\text{allowed})}{\text{max pp output current}} \qquad \ldots\ldots\ldots (4)$$

An oscillator designed using the preceding criteria is shown in Figure 3.1.6, together with the results obtained. The circuit was designed for a collector voltage swing of 2 V_{pp}, hence, from Equation (4) an effective load resistance of 400Ω is required, using the typical maximum output current of 5 mA. Figure 3.1.7 shows the output waveform, frequency stability as a function of power supply is shown in Figure 3.1.8.

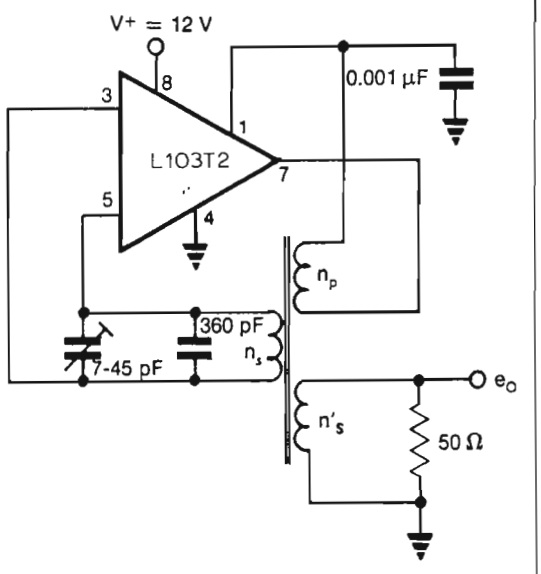


Fig. 3.1.6 – 10 MHz Oscillator

e_o = 500 mV_{pp}
f_{osc} = 10 MHz
$n_s = n_p$ = 9t 24 swg bifilar wound
n's = 4.5t 24 swg wound over n_s and n_p
Transformer assembly Neosid A7

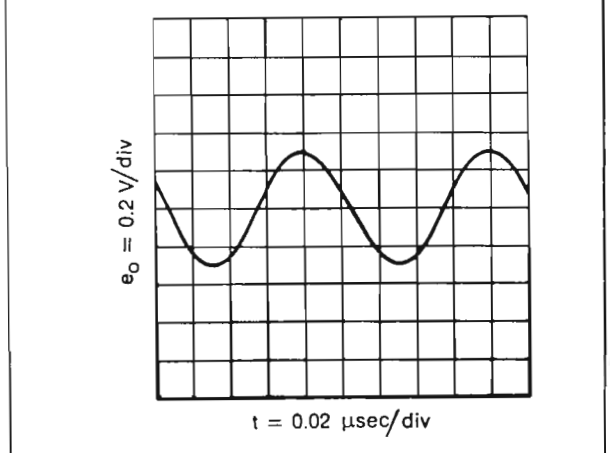


Fig. 3.1.7 – Oscillator Output Waveform

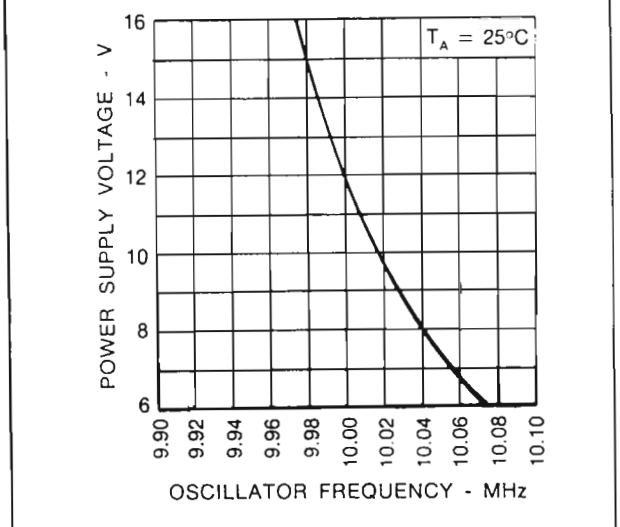


Fig. 3.1.8 – 10 MHz Oscillator Frequency Stability

3.2 L123T2 Power Supply Circuits

3.2.1 Basic Low Voltage Regulator (2 to 6.5 Volts)

This is shown in Figure 3.2.1 and is the standard low voltage configuration for positive output voltages. The use of a resistive divider on the reference voltage(V_{ref}) ensures that no attenuation of the output voltage occurs. Therefore no attenuation of changes of output voltage occurs at the input of the error amplifier. If desired the output voltage can be adjusted to a specific value by means of a potentiometer RV_1 as shown in Figure 3.2.2. Details of resistor and potentiometer values can be obtained from Table 1 for the specific value of output voltage chosen. The frequency compensation used (100 pF) assures stability with the minimum number of components. Short circuit protection is provided by R_{SC} and the transistor within the L123T2. The value of the limit current,

$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$, where $V_{SENSE} = V_{be(ON)}$ of the current limit transistor (0.7 V typical).

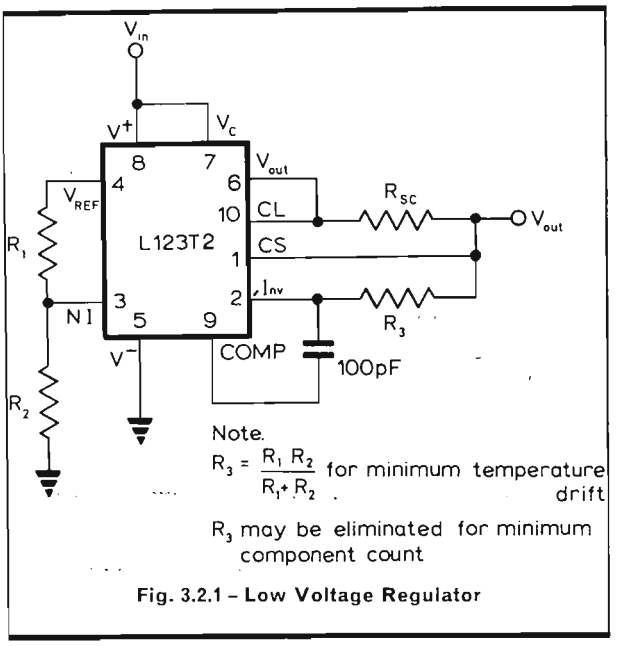


Fig. 3.2.1 – Low Voltage Regulator

Typical Performance

Regulated Output Voltage: +5 V
Line Regulation ($\Delta V_{IN} = 3$ V): 0.5 mV
Load Regulation ($\Delta I_L = 50$ mA): 1.5 mV

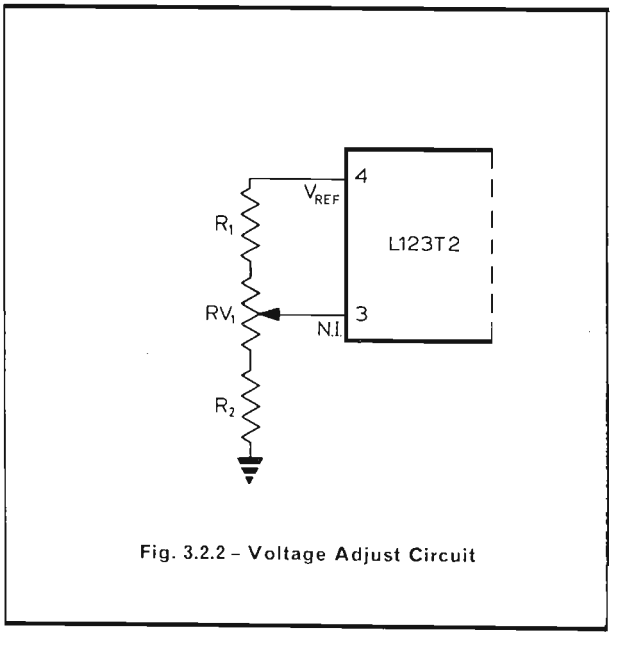


Fig. 3.2.2 – Voltage Adjust Circuit

3.2.2 Basic High Voltage Regulator (8 to 37 Volts)

This is shown in Figure 3.2.3 and is the standard high voltage configuration for positive output voltages. As the output voltage is greater than the reference voltage, the output voltage must be attenuated by R_1 and R_2. If desired, the output voltage can be set to a specific value by means of a potentiometer RV_1 as shown in Figure 3.2.4. Details of resistor and potentiometer values can be obtained from Table 1 for the specific value of output voltage chosen. The frequency compensation used (100 pF) assures stability with the minimum number of components. Short circuit protection is provided by R_{SC} and the transistor within the L123T2. The value of the limit current

$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$ where $V_{SENSE} = V_{be(ON)}$ of the current limit transistor (0.7 V typical).

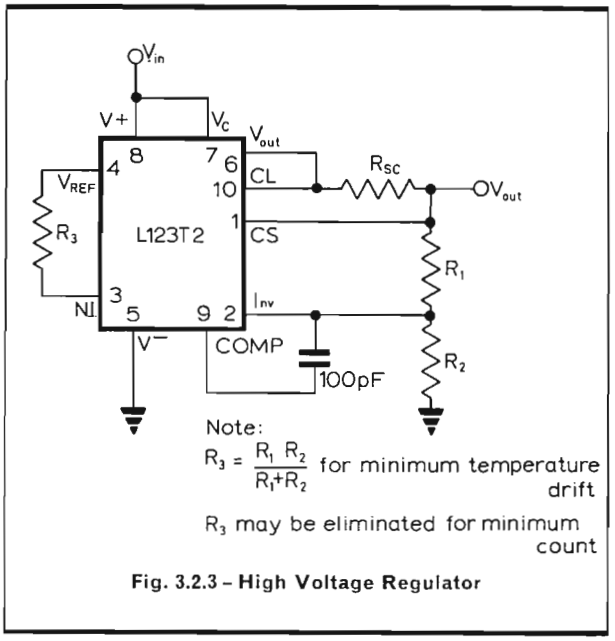


Fig. 3.2.3 – High Voltage Regulator

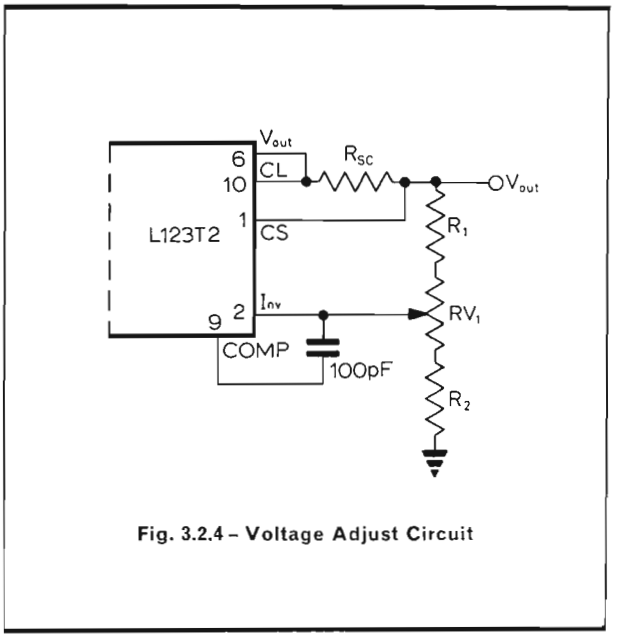


Fig. 3.2.4 – Voltage Adjust Circuit

Typical Performance

Regulated Output Voltage: +15 V
Line Regulation ($\Delta V_{IN} = 3$ V): 1.5 mV
Load Regulation ($\Delta I_L = 50$ mA): 4.5 mV

3.2.3 Positive Voltage Regulator (External NPN Pass Transistor) (8 to 37 Volts)

The circuit shown in Figure 3.2.5 is similar to that described in Section 3.2.2 but uses an external NPN transistor as the series element. Therefore higher values of load current may be drawn. The circuit operation is similar to that of 3.2.2. The larger value of frequency compensation capacitor (500 pF) is to allow for the external transistor.

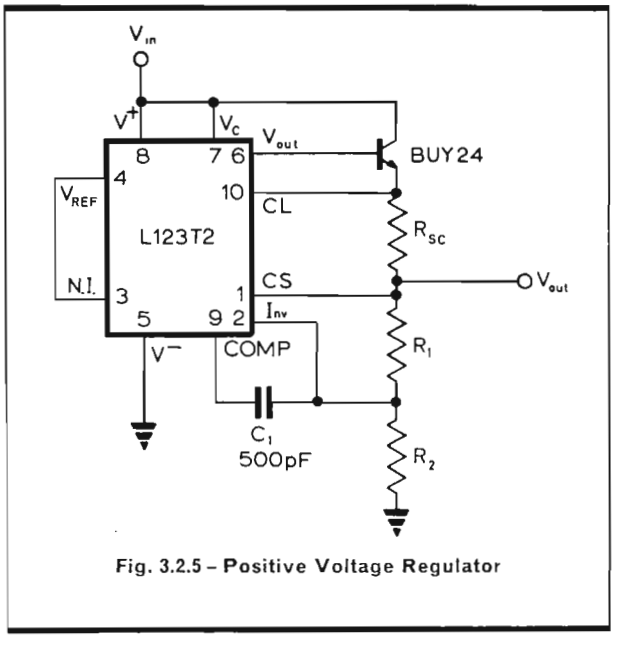


Fig. 3.2.5 – Positive Voltage Regulator

Typical Performance

Regulated Output Voltage: +15 V
Line Regulation ($\Delta V_{IN} = 3$ V): 1.5 mV
Load Regulation ($\Delta I_L = 1$A): 1.5 mV

3.2.4 Regulator with High Power Supply Rejection

Where short circuit protection of the output is not required the internal current limit transistor may be used to increase the power supply rejection ratio. Using the connection shown in Figure 3.2.6 power supply rejection ratios as high as 100 dB (100,000:1) may be achieved. The base/emitter junction of the current limit transistor is reverse biased and used as a zener diode to provide V+ with a stable input voltage. It should be noted that the zener current must not exceed 5 mA. The circuit shown in Figure 3.2.6 is a low voltage regulator and that shown in Figure 3.2.7 a high voltage version.

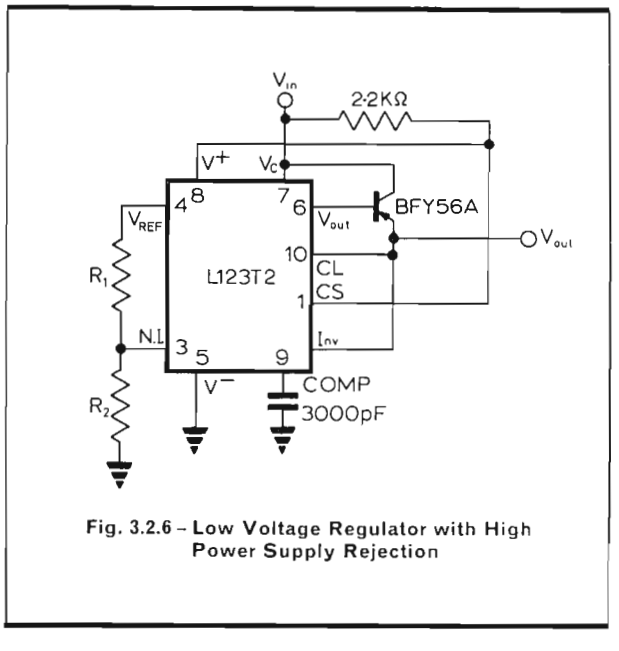


Fig. 3.2.6 – Low Voltage Regulator with High Power Supply Rejection

Typical Performance

Regulated Output Voltage: +5 V
Line Regulation ($\Delta V_{IN} = 15$ V): 1 mV
Load Regulation ($\Delta I_L = 50$ mA): 1 mV

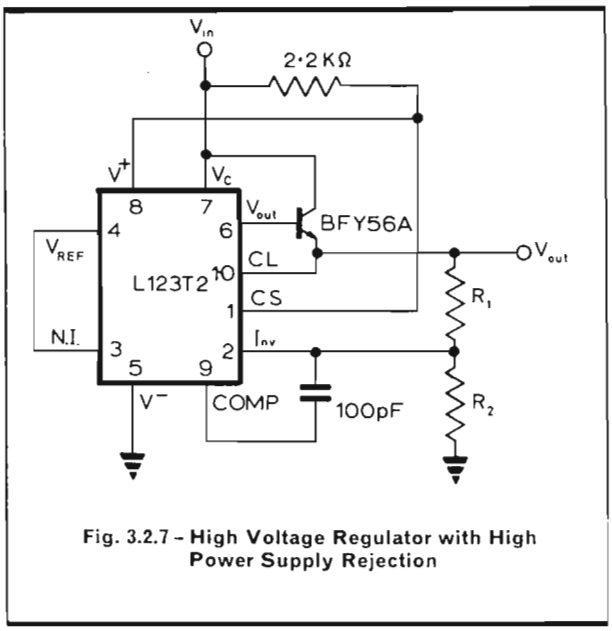


Fig. 3.2.7 – High Voltage Regulator with High Power Supply Rejection

Typical Performance

Regulated Output Voltage: +15 V
Line Regulation ($\Delta V_{IN} = 15$ V): 1 mV
Load Regulation ($\Delta I_L = 50$ mA): 10 mV

3.2.5 Negative Voltage Regulator (—9 to —40 Volts)

This is shown in Figure 3.2.8 and uses an external PNP series pass element. As the L123T2 is supplied by the regulated output voltage, the maximum input voltage is limited by the breakdown voltage of the PNP series pass transistor.

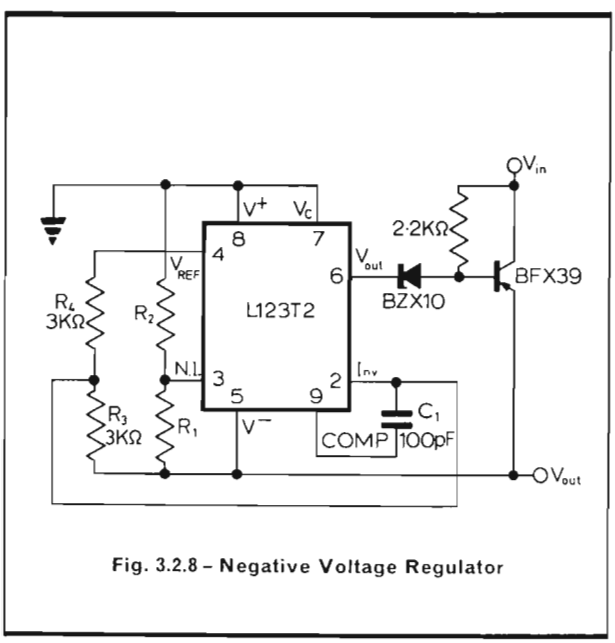


Fig. 3.2.8 – Negative Voltage Regulator

Typical Performance

Regulated Output Voltage: —15 V
Line Regulation ($\Delta V_{IN} = 3$ V): 1 mV
Load Regulation ($\Delta I_L = 100$ mA): 2 mV

3.2.6 Negative Voltage Regulator (Low Voltage Version)

This is shown in Figure 3.2.9 and uses an external PNP series pass element. The L123T2 requires a minimum applied voltage of 9.5 Volts to ensure satisfactory operation. Therefore when regulating negative voltages less than 9 V it is necessary to connect the device, as shown, to a positive supply such that the voltage across the device is always greater than 9.5 Volts.

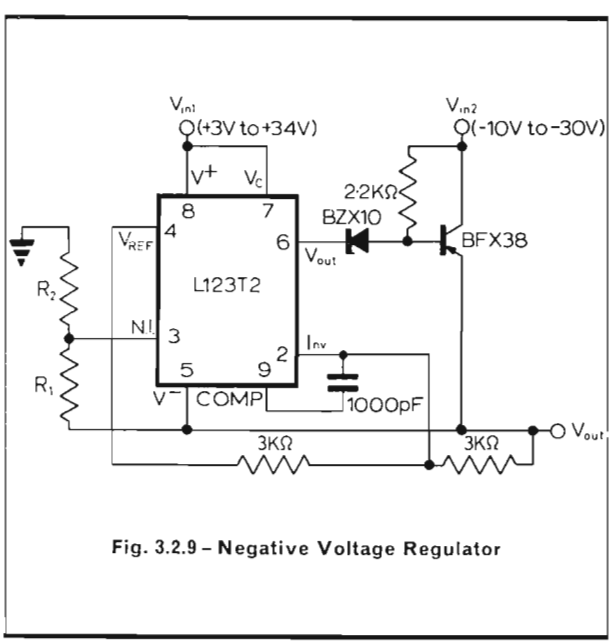


Fig. 3.2.9 – Negative Voltage Regulator

Typical Performance

Regulated Output Voltage: —6 V
Line Regulation ($\Delta V_{IN} = 10$ V): 4 mV
Load Regulation ($\Delta I_L = 100$ mA): 2 mV

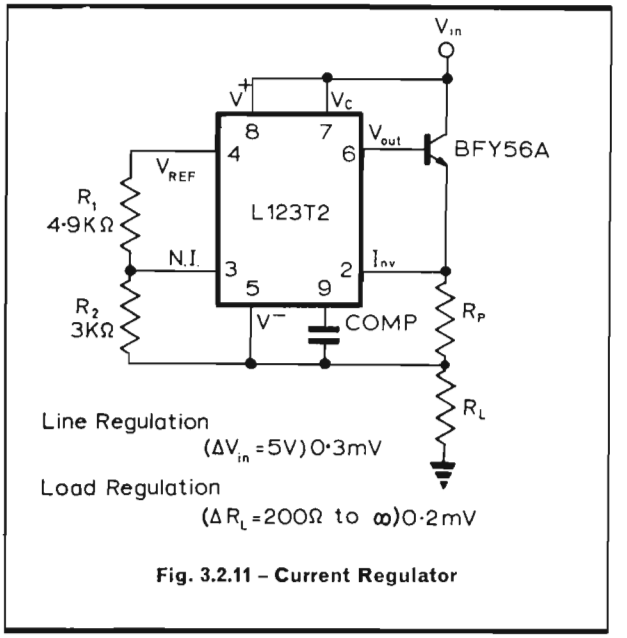


Fig. 3.2.11 – Current Regulator

3.2.8 Current Regulator

This is shown in Figure 3.2.11 where $I_{out} = \frac{3}{R_p}$

(where Rp is in Ω). The line regulation will deteriorate with programmed currents under 10 mA as both the programmed current and the quiescent current flow through the load.

3.2.9 Shunt Regulator

Shunt regulation may be achieved as shown in Figure 3.2.12. Care must be taken in calculating the power dissipation of the current limiting resistor, as this is the only passive component which dissipates a high power (excluding the load).

3.2.7 Positive Low Voltage Regulator with remote shut down

This is shown in Figure 3.2.10 and uses an external NPN transistor. The transistor is switched on by a CCSL 'high' input level and shuts the regulator off. Where current limiting is not required the BFY 56A may be replaced by the internal current limiting transistor. If this is done the C_L pin is grounded and the C_S pin should be driven with approximately 1 mA of base current.

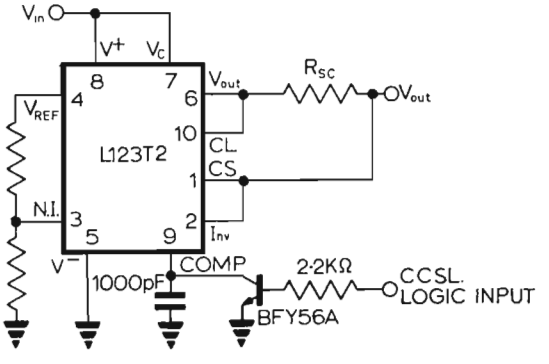


Fig. 3.2.10 – Positive Low Voltage Regulator with Remote Shutdown

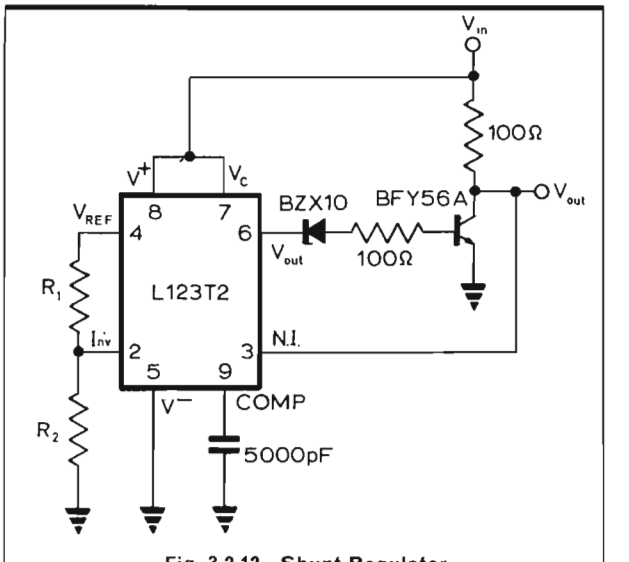


Fig. 3.2.12 – Shunt Regulator

Typical Performance

Regulated Output Voltage: +5 V
Line Regulation ($\Delta V_{IN} = 3$ V): 0.5 mV
Load Regulation ($\Delta I_L = 50$ mA): 1.5 mV

Typical Performance

Regulated Output Voltage: +5 V
Line Regulation ($\Delta V_{IN} = 10$ V): 2 mV
Load Regulation ($\Delta I_L = 100$ mA): 5 mV

TABLE 1
RESISTOR VALUES IN KΩ FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Adjustable Output ±10%		
		R_1	R_2	R_1	RV_1	R_2
+3	3.2.1, 3.2.6, 3.2.12	4.12	3.01	1.8	0.5	1.2
+3.6	3.2.1, 3.2.6, 3.2.12	3.57	3.65	1.5	0.5	1.5
+5	3.2.1, 3.2.6, 3.2.12	2.15	4.99	0.75	0.5	2.2
+6	3.2.1, 3.2.6, 3.2.12	1.15	6.04	0.5	0.5	2.7
+9	3.2.3, 3.2.5, 3.2.7	1.87	7.15	0.75	1.0	2.7
+12	3.2.3, 3.2.5, 3.2.7	4.87	7.15	2.0	1.0	3.0
+15	3.2.3, 3.2.5, 3.2.7	7.87	7.15	3.3	1.0	3.0
+28	3.2.3, 3.2.5, 3.2.7	21.0	7.15	5.6	1.0	2.0
Negative Output Voltage	**Applicable Figures**	**Fixed Output ±5%**		**Adjustable Output ±10%**		
		R_1	R_2	R_1	RV_1	R_2
−6	3.2.9	3.57	2.43	1.2	0.5	0.75
−9	3.2.8	3.48	5.36	1.2	0.5	2.0
−12	3.2.8	3.57	8.45	1.2	0.5	3.3
−15	3.2.8	3.65	11.5	1.2	0.5	4.3
−28	3.2.8	3.57	24.3	1.2	0.5	10

ADDITIONAL FORMULAE

Short circuit current $I_{LIMIT} = \dfrac{0.7}{R_{SC}(\Omega)}$

Figure 3.2.1 and 3.2.6 $V_{OUT} = \dfrac{R_1}{R_1+R_2} \times 7 \text{ Volts}$

where $(R_1+R_2) > 1.5K\Omega$

Figure 3.2.3, 3.2.5, 3.2.7 $V_{OUT} = \dfrac{R_1+R_2}{R_2} \times 7 \text{ Volts}$

Figure 3.2.9 and 3.2.8 $V_{OUT} = \dfrac{3.5(R_1+R_2)}{R_1} \text{ Volts}$

3.3 L127T2 Basic Circuits

3.3.1 Low Drift Operational Amplifier

The L127T2 may be used with an integrated circuit operational amplifier to achieve a low drift (0.6μV/°C typical) and high input resistance (300 MΩ typical). Such an arrangement is shown in Figure 3.3.1 where the drift of the post amplifier is negligible. For example, a μA709 having maximum drifts of 10μV/°C and 2nA/°C will only contribute 0.11μV/°C to the drift of the overall amplifier.

In order to achieve optimum drift performance several points must be considered. Firstly, since the L127T2 must regulate its power dissipation to maintain a constant chip temperature, best control is achieved if the case to ambient thermal resistance is kept as high as possible. Therefore a heat sink should not be fitted to the device and moving air over the circuitry should be minimised. Secondly, thermo-electric effects produced by two dissimilar metals in contact should be considered. These can occur when component leads are soldered to a copper printed circuit board. In order to minimise this the junctions should be kept at the same temperature by keeping them physically close and preventing unequal air movement or heat sinking.

The methods of nulling the input offset voltage and achieving the frequency compensation can be obtained by referring to section 2.3.2. The value of R_{adj} can be found by referring to Figure 2.3.8.

This composite 'Low Drift Operational Amplifier' may be used in a variety of applications including many of the circuits given in 'the application of linear microcircuits', volume 1.

3.3.2 High Performance Voltage Follower

An example of a voltage follower is given in Section 3.4.1 using a L141T2. Where higher performance is required the circuit shown in Figure 3.3.2 may be used. This gives an input offset voltage drift of 0.6μV/°C and an input offset current drift of 15 pA/°C. The input impedance is 2,000 MΩ and the maximum input voltage range is ±12 V. Because of the high value of open loop gain (134 dB) the closed loop gain is well defined at unity (0 dB) and the output impedance very low.

3.3.3 Precision Integrator

In many fields of electronics integrators using operational amplifiers with a capacitor in the feedback loop are used. High performance can be obtained, but where long time constants are required the input resistance of the operational amplifier is often too low (e.g. μA709, $R_{in} \simeq 250$ KΩ). This can be overcome by using the L127T2 with its high input resistance and low drift. A practical circuit is shown in Figure 3.3.3 having an output error of 0.01%/Volt/°C.

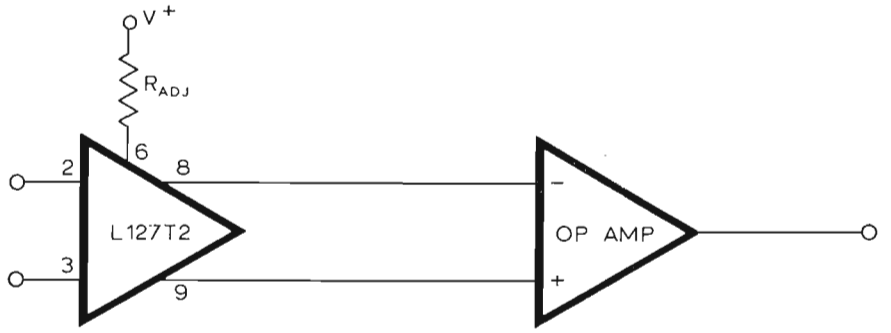


Fig. 3.3.1 – Low Drift Operational Amplifier

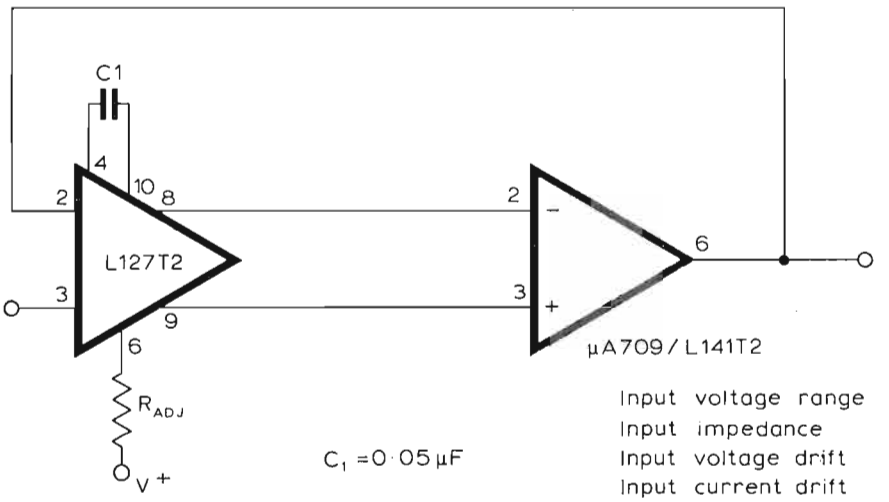


Fig. 3.3.2 – High Performance Voltage Follower

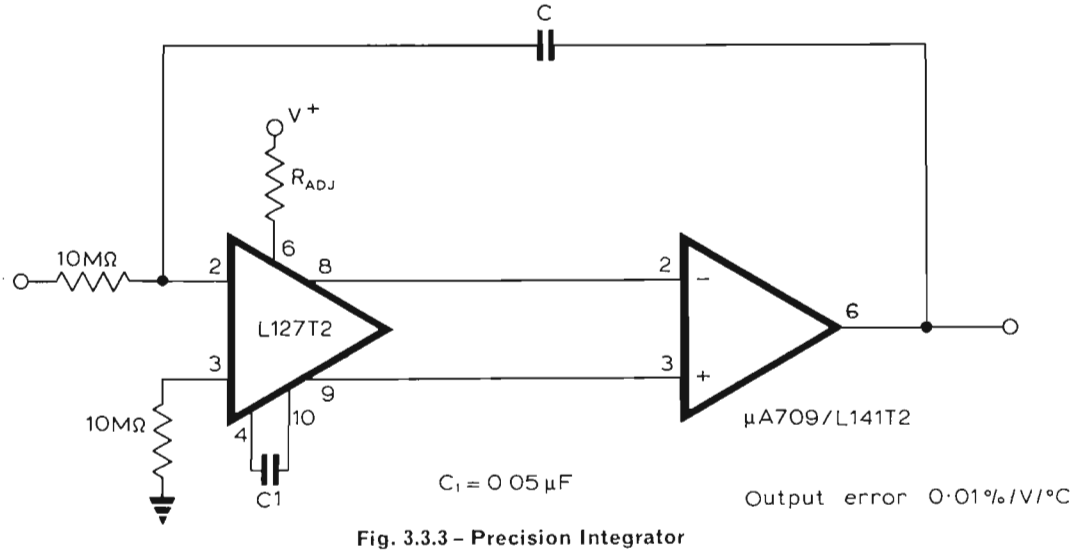


Fig. 3.3.3 – Precision Integrator

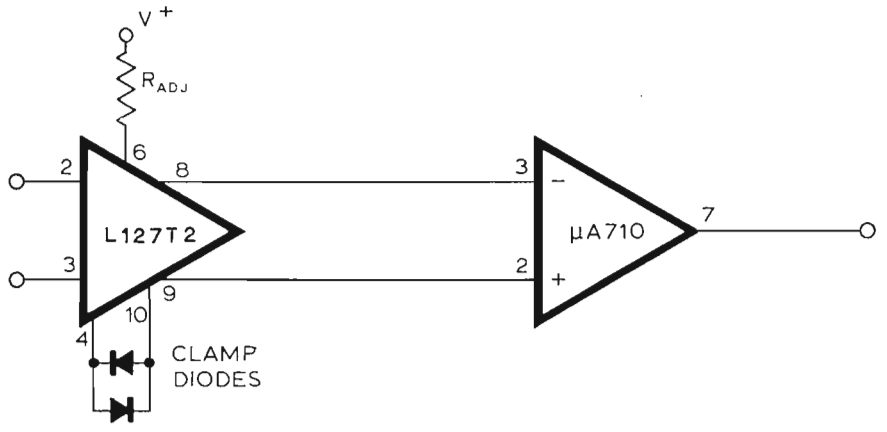


Fig. 3.3.4 – High Input Resistance Comparator

3.3.4 High Input Resistance Comparator

Where a voltage comparator that presents negligible loading is required and/or where low drift is required, the L127T2 may be used. A typical circuit is shown in Figure 3.3.4 and has the following performance.

Input Voltage Range	±8 V
Differential Input Voltage Range	±10 V (maximum)
Input Resistance	300 MΩ
Voltage Gain	170,000

3.4 L141T2 Basic Circuits

3.4.1 Voltage Follower

This is shown in Figure 3.4.1 and is frequently used as a buffer amplifier to reduce error caused by source loading to isolate high resistance (or high impedance) sources from the following circuitry. The output voltage duplicates, or follows, the input voltage, hence the name voltage follower.

The voltage follower is a worst case application for an operational amplifier for two reasons:

(1) The maximum amount of negative feedback is applied, normally necessitating external frequency compensation components to reduce the gain at high frequencies to unity to ensure stability. The L141T2 does not require such components owing to its internal frequency compensation network.

(2) The voltage follower is subject to a condition known as latch up ('the application of linear microcircuits', volume 1, Section 2.6.2). This occurs if the common mode input voltage limit is exceeded. As explaind earlier, the input stage of the L141T2 has been designed to prevent latch up from occurring.

The accuracy of the voltage follower is determined by the operational amplifier's open loop voltage gain and common mode rejection ratio.

The expression for accuracy is:

$$\frac{E_{out}}{E_{in}} = \frac{1 + \frac{1}{CMRR}}{1 + \frac{1}{A_o}}$$

where CMRR is the common mode rejection ratio expressed as a ratio and A_o is the open loop voltage gain.

Using typical figures for the L141T2 the d.c. accuracy of the voltage is found to be better than 0.003 per cent.

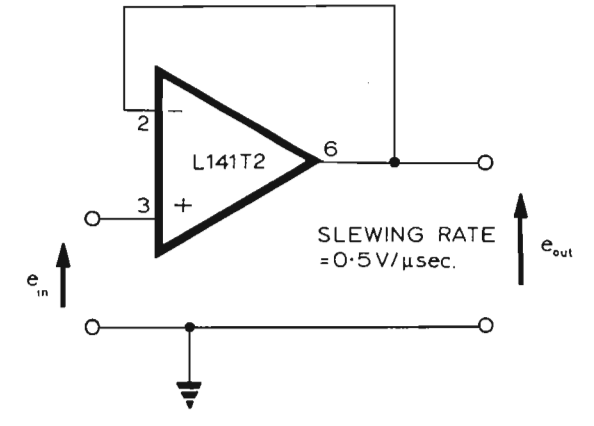


Fig. 3.4.1 – Voltage Follower

3.4.2 Integrator

The integrator, shown in Figure 3.4.2, provides an output that is proportional to the time integral of the input signal. Although it may not be immediately obvious, the integrator, if it is to operate reliably, requires both large common mode and differential mode input voltage ranges. There are several ways that the input voltage limits may be exceeded. The most obvious is that transients occurring at the output of the amplifier can be fed back to the input via the integrating capacitor C_1. Therefore, either the common mode or the differential input voltage limits can be exceeded. Another dangerous condition can occur when the integrator is driven from fast rising or falling input signals (e.g. square waves). The output of the amplifier cannot respond instantaneously owing to the finite value of slewing rate. Therefore, during the period before the output changes, the summing point at pin 2 of the amplifier may not be held at ground potential. If the input voltage change is large enough, the voltage at the summing point could exceed the safe limits for the amplifier.

The L141T2 is more resistant to this type of damage because of its large differential and common mode input voltage ranges.

The transfer function for the integrator is given by:

$$E_{out} = -\frac{1}{R_1.C_1}\int E_{in}\,dt$$

For example, let the response of the integrator to a symmetrical square wave input be considered. If the input has a peak amplitude of A volts, a period of T, then the peak to peak output can be calculated by integrating over one-half of the input period.

$$\left|E_{out}\right|_{pk\text{-}pk} = \frac{1}{R_1.C_1}\int_0^{T/2} A.dt$$

$$= \frac{A}{R_1.C_1}\left(\frac{T}{2}\right) \text{ volts}$$

The waveshape, at the output, will be triangular corresponding to the integral of a square wave. For the component values in Figure 3.4.2 and assuming A=5 volts and T=1 mSec,

$$E_{out}{}_{pk\text{-}pk} = \frac{5}{10^4.0{\cdot}1.10^{-6}}\left(\frac{10^{-3}}{2}\right)$$

$$= 2.5 \text{ volts peak to peak.}$$

The resistor R_2 is included to provide d.c. stabilisation for the integrator. Its function is to limit the d.c. gain of the amplifier and thus minimise drift. The frequency above which the circuit will function as an integrator is given by:

$$f^1 = \frac{1}{2\pi.R_2.C_1} \text{ Hz}$$

For optimum linearity, the frequency of the input signal should be >10 times f^1. The linearity of the circuit shown in Figure 3.4.2 is better than 1 per cent for an input having a frequency of 1 kHz.

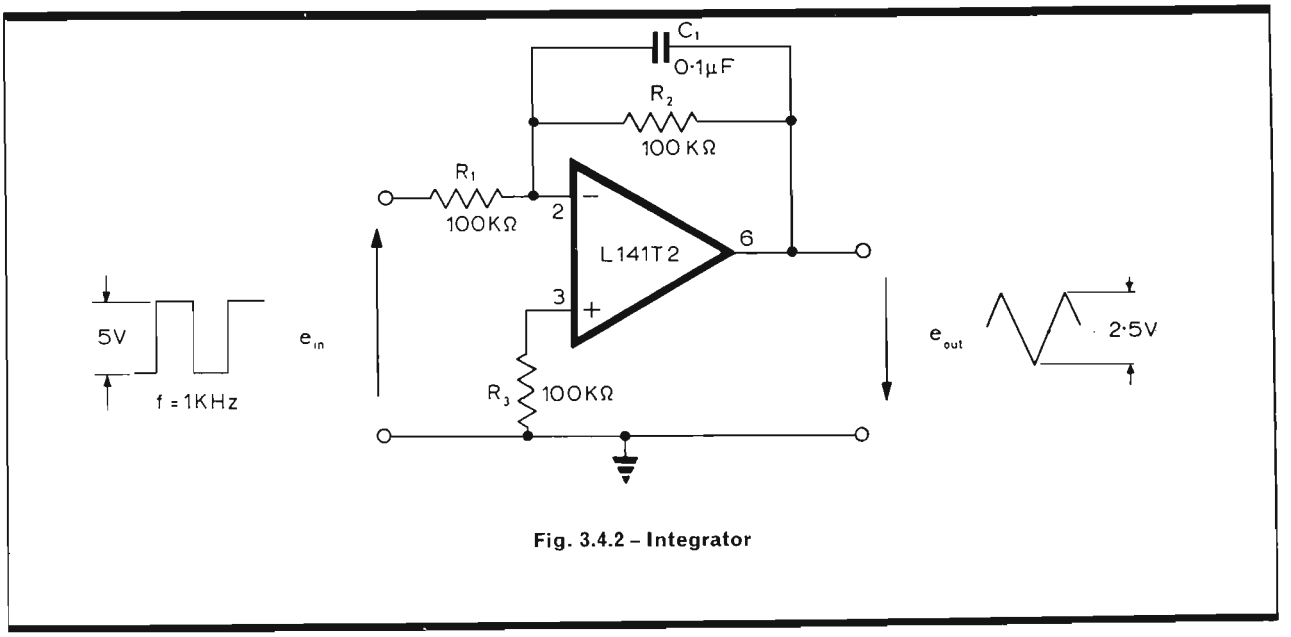


Fig. 3.4.2 – Integrator

3.4.3 Differentiator

The differentiator circuit, shown in Figure 3.4.3, provides an output proportional to the derivative of the input signal. As with the integrator, the differentiator is subject to damage from fast rising input signals. Again the wide input voltage ranges of the L141T2 offer improved resistance to damage.

The transfer function for the differentiator is given by:

$$E_{out} = -R_2.C_1 . \frac{de_{in}}{dt}$$

Since the differentiator performs the reverse of the integrator function, a triangular input will produce a square wave output. For the circuit in Figure 3.4.3 and a triangular wave of 2.5 volts peak to peak with a period of 1 mSec,

$$\frac{de_{in}}{dt} = \frac{2.5 \text{ volts}}{0.5\text{mSec}} = 5 \frac{\text{volts}}{\text{mSec}}$$

$$\therefore E_{out} = -(10^4.0{\cdot}1.10^{-6})\, 5 \frac{\text{volts}}{\text{mSec}}$$

$E_{out} = 5$ volts peak to peak

The resistor R_1 is necessary to limit the high frequency gain of the differentiator. It makes the circuit less susceptible to high frequency noise and ensures dynamic stability. The corner frequency where the gain limiting comes into effect is given by:

$$f^1 = \frac{1}{2\pi.R_1.C_1}$$

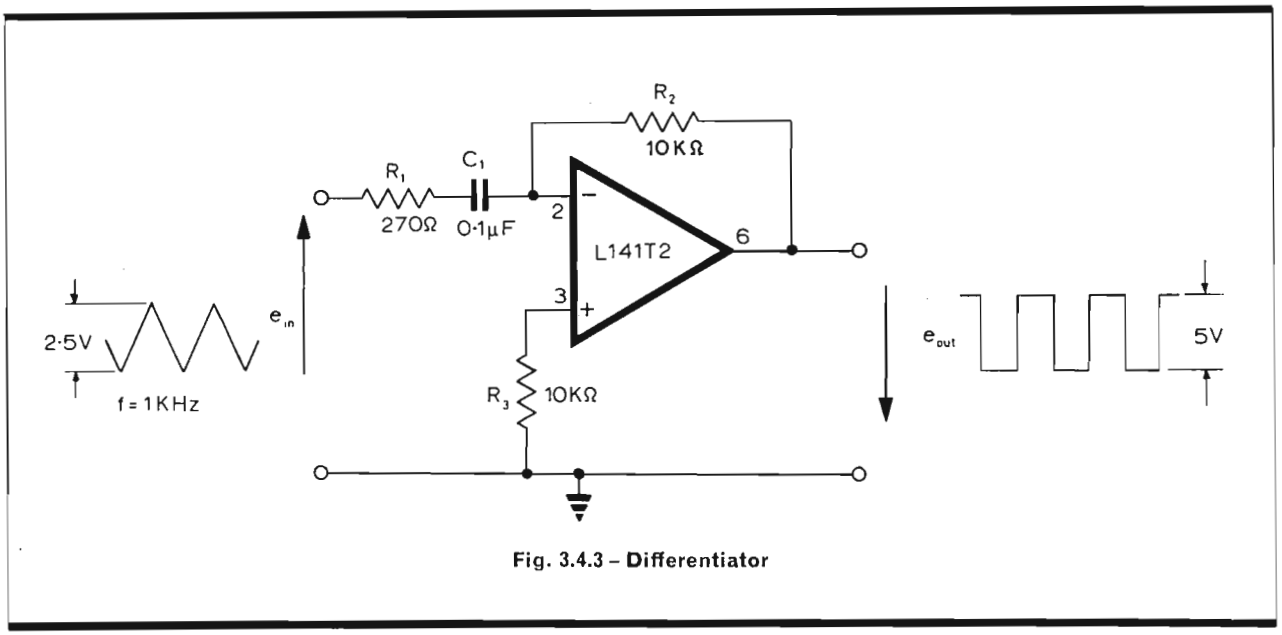


Fig. 3.4.3 – Differentiator

For accurate operation f^1 should be >10 times the highest input frequency. A maximum value for the corner frequency (f^1) is determined by the stability criteria. In general, it should be no greater than the geometric mean between $\frac{1}{2\pi.R_2.C_1}$ and the gain bandwidth product of the operational amplifier. The L141T2 has a gain bandwidth product of approximately 1 MHz, therefore the limit on f^1 is given by:

$$f^1 < \sqrt{\frac{10^6}{2\pi.R_2.C_1}}$$

3.4.4 Inverting Amplifier

The inverting amplifier, as shown in Figure 3.4.4, is one of the most suitable connections where high accuracy and low distortion are required. This is because the amplifier does not see any large signal swings at its input. It is also the most suitable configuration for summing applications as the summing junction is a virtual earth, giving good isolation between the inputs. However, the input resistance is low compared to the non-inverting configuration, being approximately equal to R_{in}.

A summary of the performance is given below.

3.4.5 Non-Inverting Amplifier

The non-inverting configuration, as shown in Figure 3.4.5, is particularly useful in applications where high input impedances are required. For closed loop gains of less than about 50 dB, the input impedance is dominated by the common mode input impedance, which is typically 200 MΩ. Common mode input impedance is defined as the

Gain	R_{IN}	R_f	Typical Bandwidth	Input Resistance
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

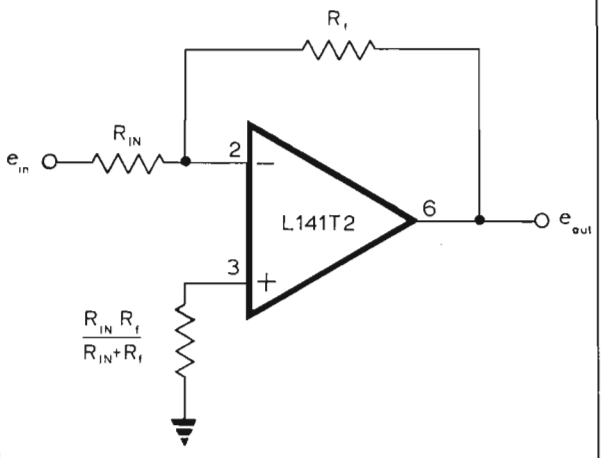


Fig. 3.4.4 – Inverting Amplifier

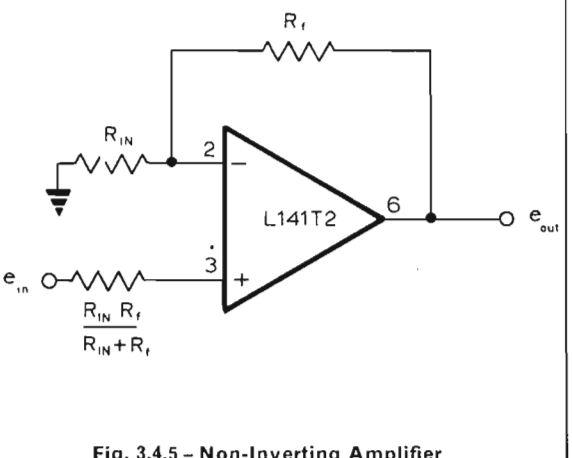


Fig. 3.4.5 – Non-Inverting Amplifier

Gain	R_{IN}	R_f	Typical Bandwidth	Input Impedance
1	∞	0	1 MHz	400 MΩ
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	100 kΩ	1 kHz	80 MΩ

parallel sum of the impedances from each input to earth. In the voltage follower mode, only one of these impedances is seen, hence the 400 MΩ in the table below. A summary of the performance is given below:

3.4.6 Clipping Amplifier

It is occasionally necessary to limit the output voltage swing of an amplifier to a specific value. This can be achieved by adding non-linear elements to the feedback network as shown in Figure 3.4.6. The zener diodes rapidly reduce the gain of the amplifier if the output voltage tries to exceed the limits set by the zener voltages. When the zener diodes are not conducting the voltage gain is determined by the resistors R_1 and R_2.

It can easily be overlooked that such an amplifier must be frequency compensated for a closed loop gain of unity. This is because the gain of the circuit falls to unity when the zener diodes commence conducting. The L141T2 is suitable, without

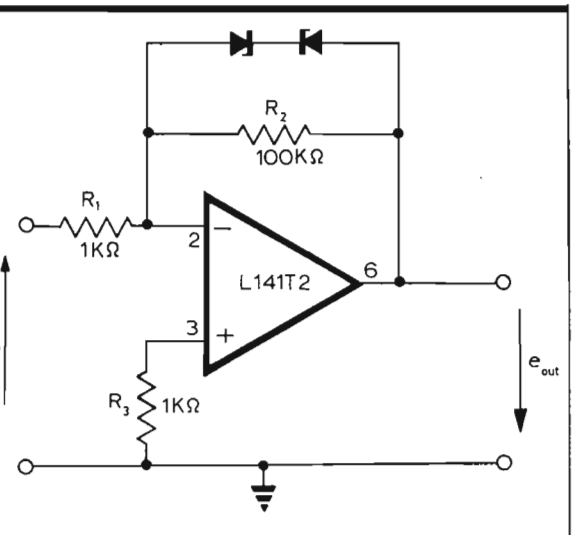


Fig. 3.4.6 – Clipping Amplifier

the need for any external components, because of its internal 'unity gain' frequency compensation.

3.4.7 Voltage Comparator

Many applications arise where a comparison must be made between two voltages and an output supplied indicating which is the greater. The L141T2 can be used as a comparator in many applications where high speed is not essential. It cannot compete with comparators designed for high speed operation (e.g. SGS μA710) as the internal compensation network limits the response time. The features that make the L141T2 attractive as a comparator are its large common mode and differential input voltage ranges. The input signals to be compared may vary over a wide range without the necessity of external protective circuitry.

A typical comparator circuit is shown in Figure 3.4.7. The zener voltage may be selected so that the output voltage is compatible with high level logic, MOS logic or normal CCSL logic thresholds.

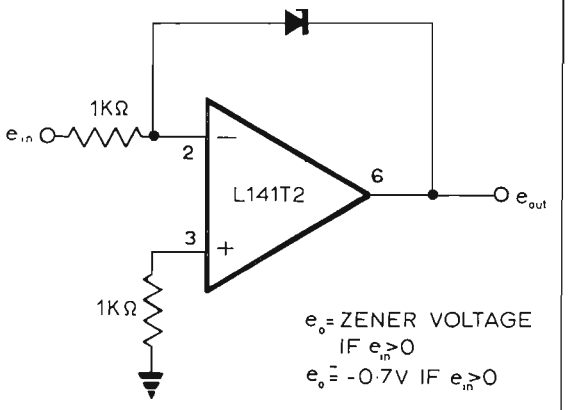


Fig. 3.4.7 – Voltage Comparator

3.4.8 Voltage Regulator Amplifier

Operational amplifiers are frequently used as reference amplifiers in voltage regulated power supplies. A typical circuit with variable output voltage is shown in Figure 3.4.8. The purpose of the amplifier is to isolate the voltage reference (a zener or temperature compensated (TC) reference diode) from changes in loading at the supply output. This ensures a lower output impedance and therefore improved load regulation. Also, because of the high gain of the L141T2, the voltage applied to the inverting input from the output voltage divider is always maintained to within a few millivolts of the reference voltage. The output voltage can be adjusted by changing the division ratio of the divider. The 800 KΩ input resistance of the L141T2 keeps loading of the reference zener diode to a minimum. The output resistance of the circuit is less than 0.1Ω.

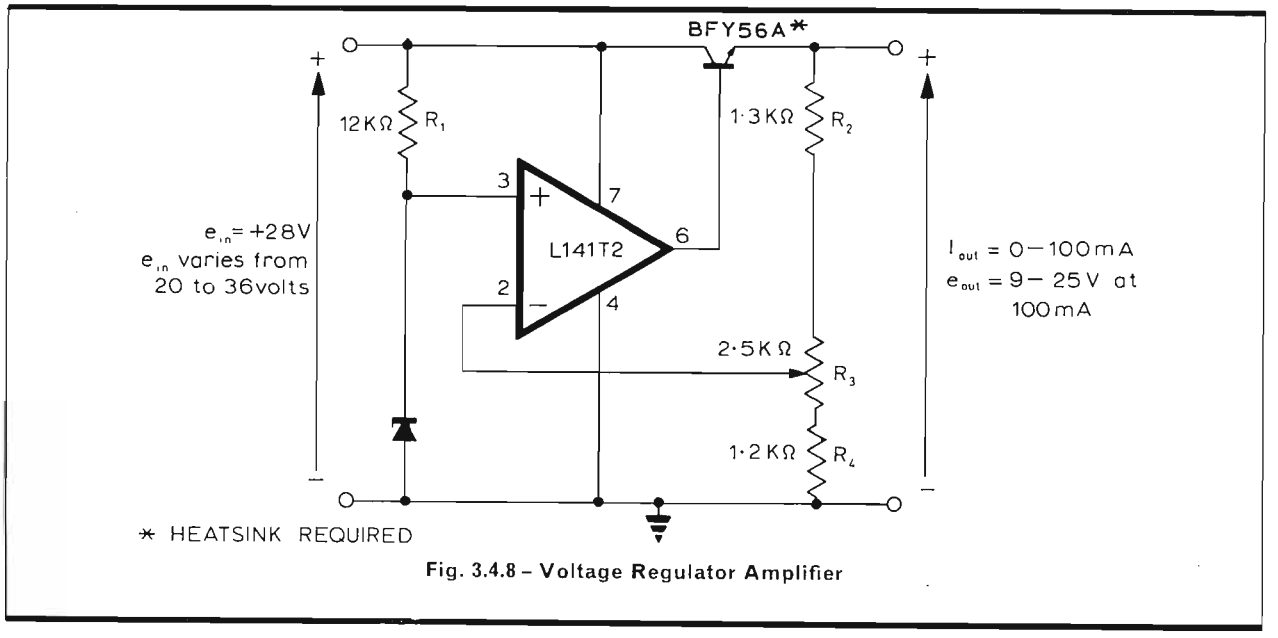


Fig. 3.4.8 – Voltage Regulator Amplifier